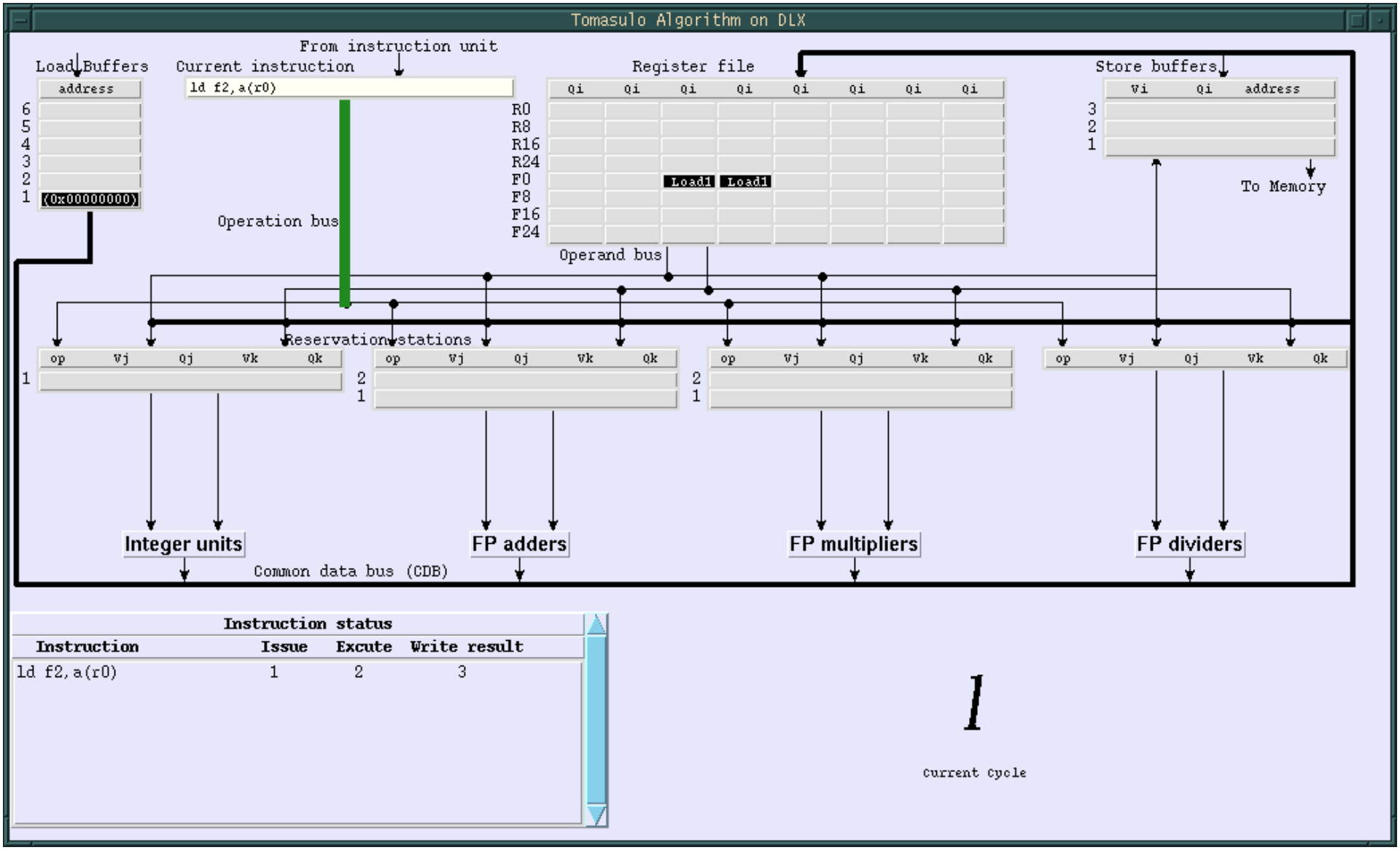
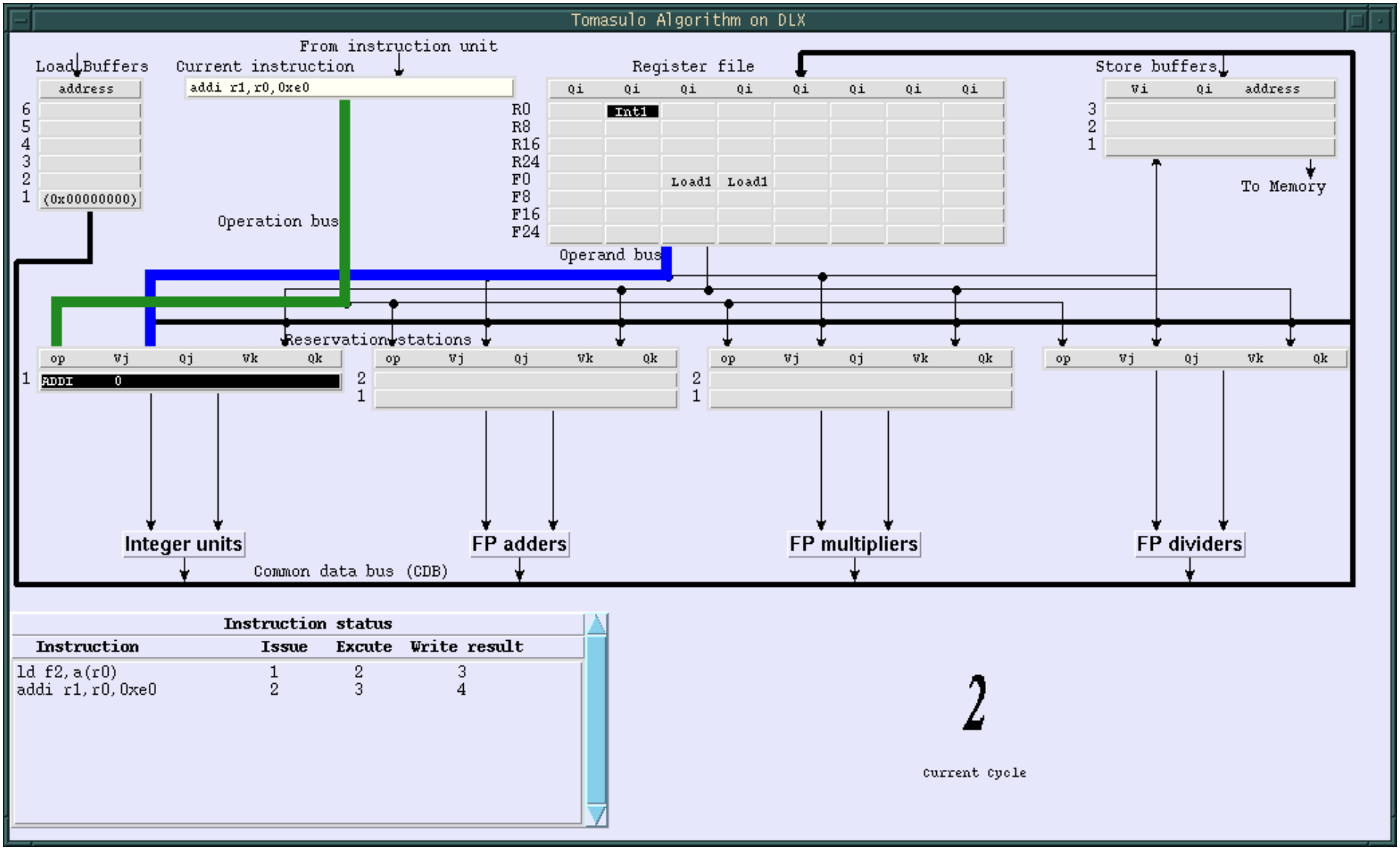
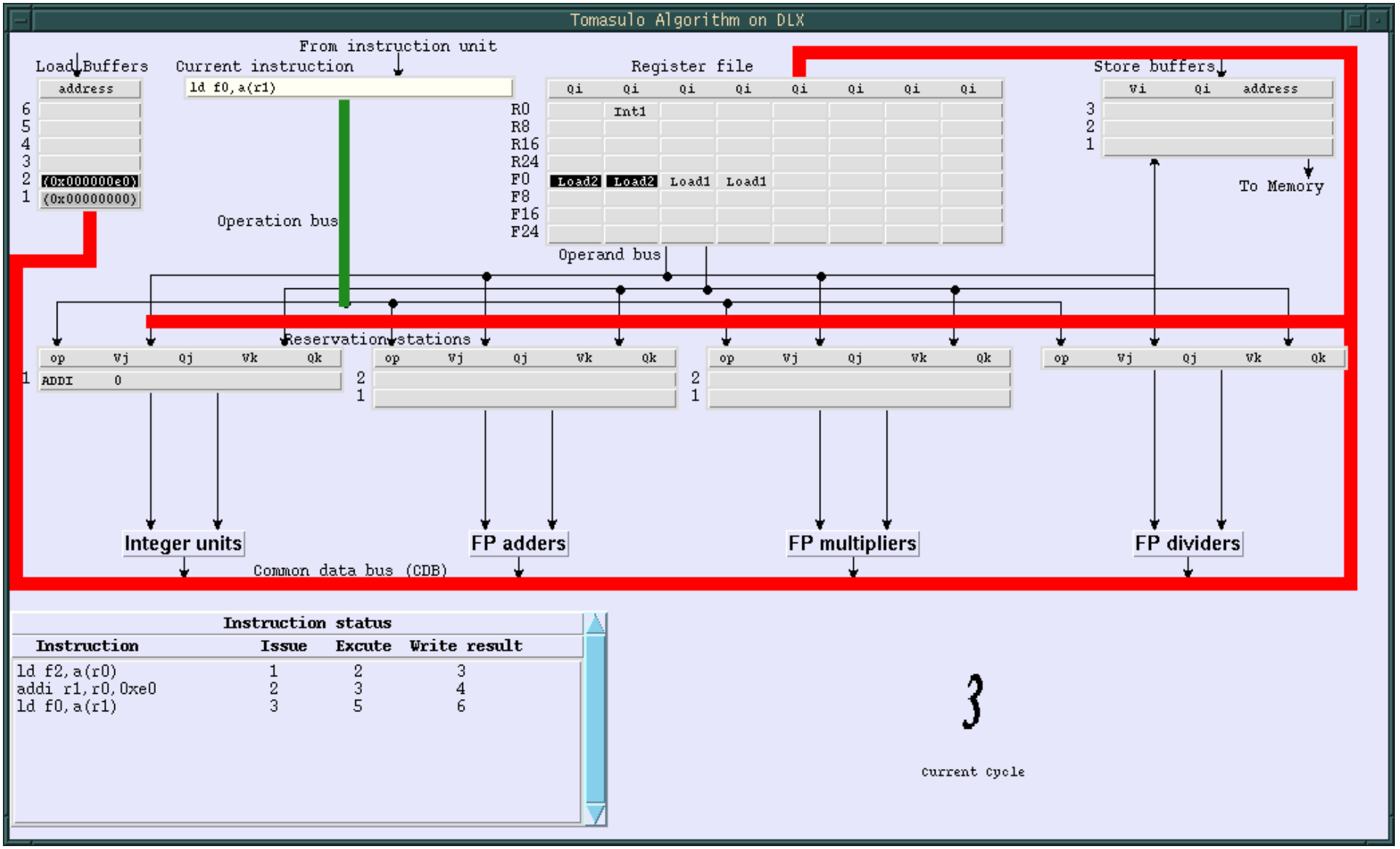
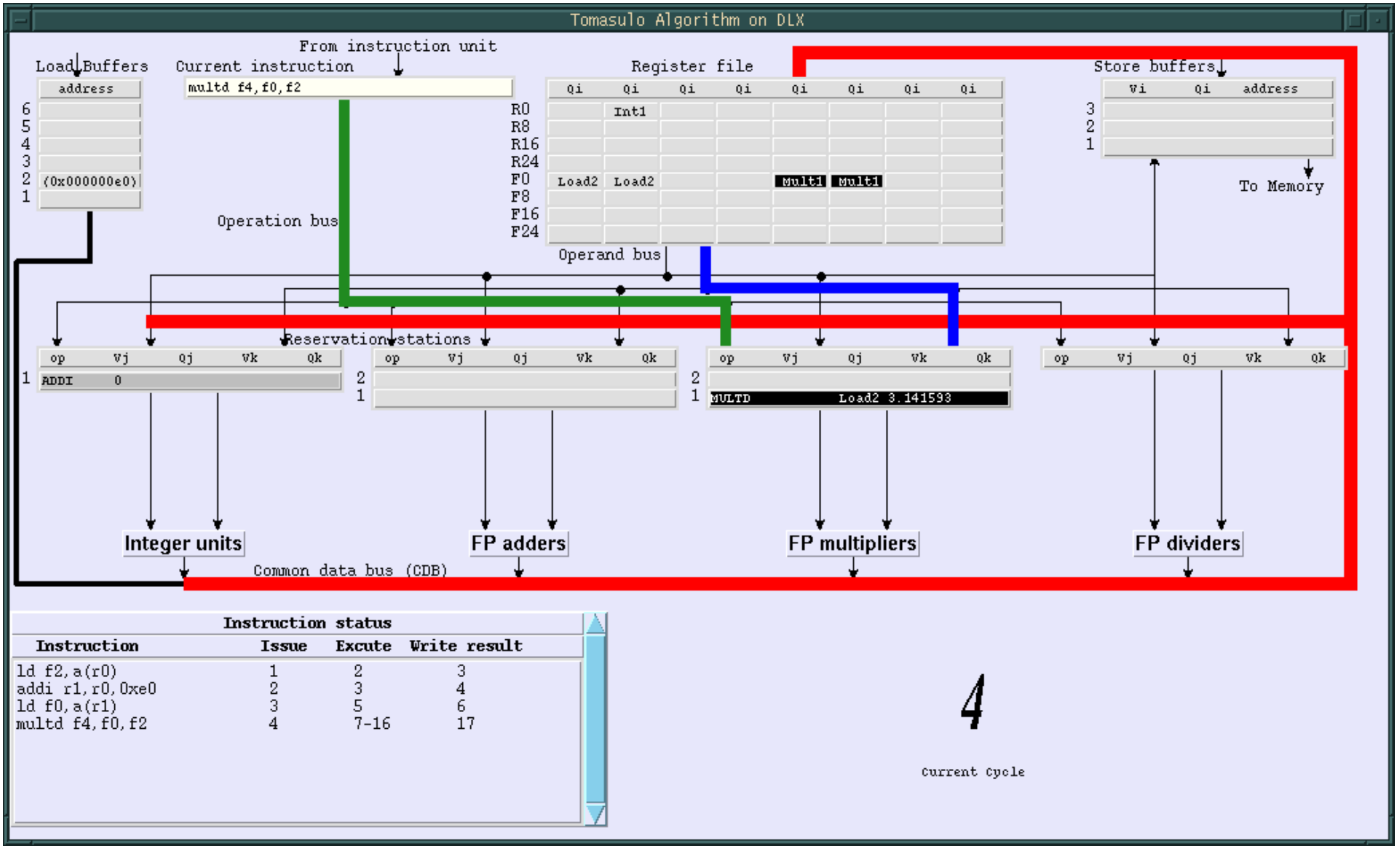
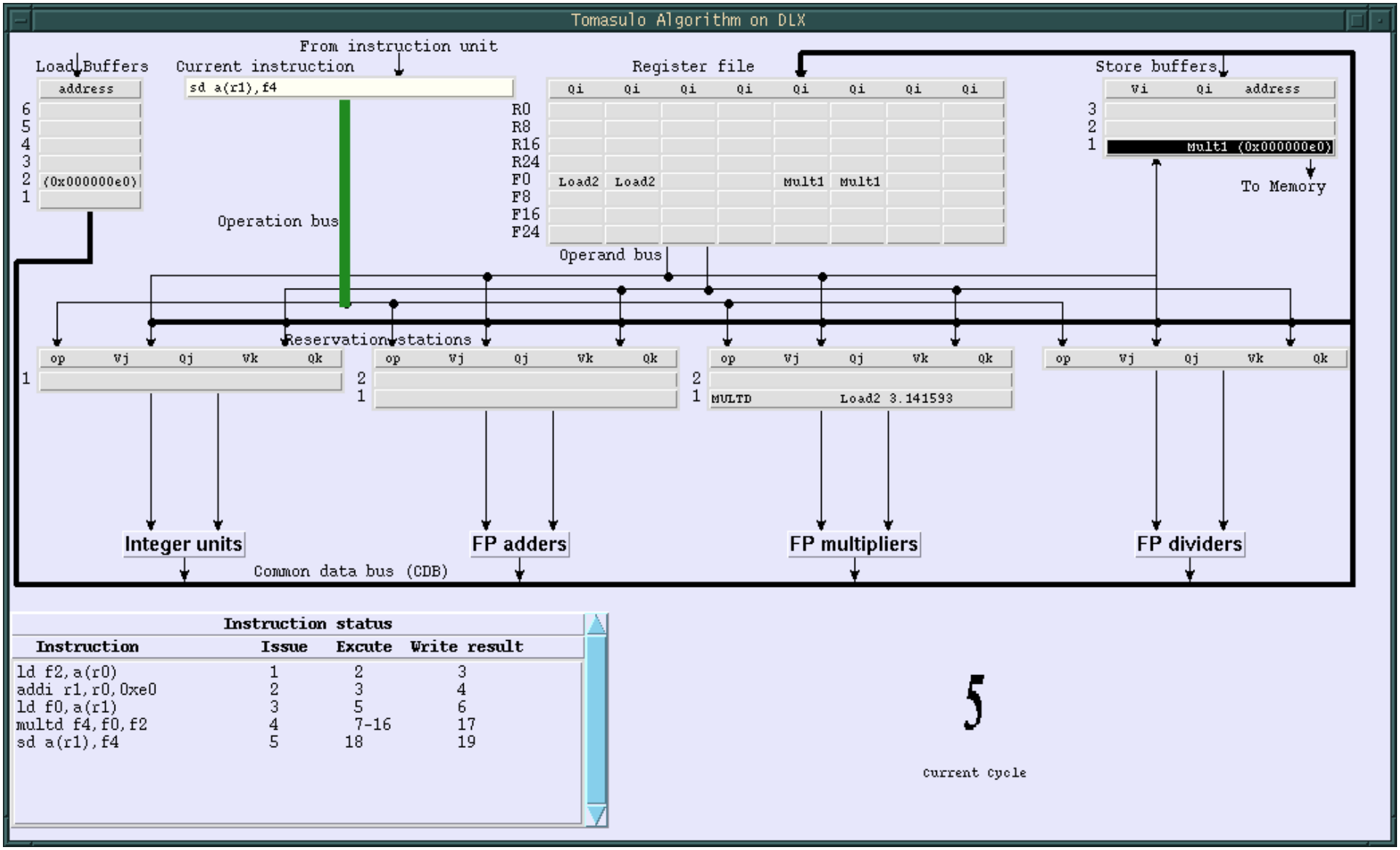
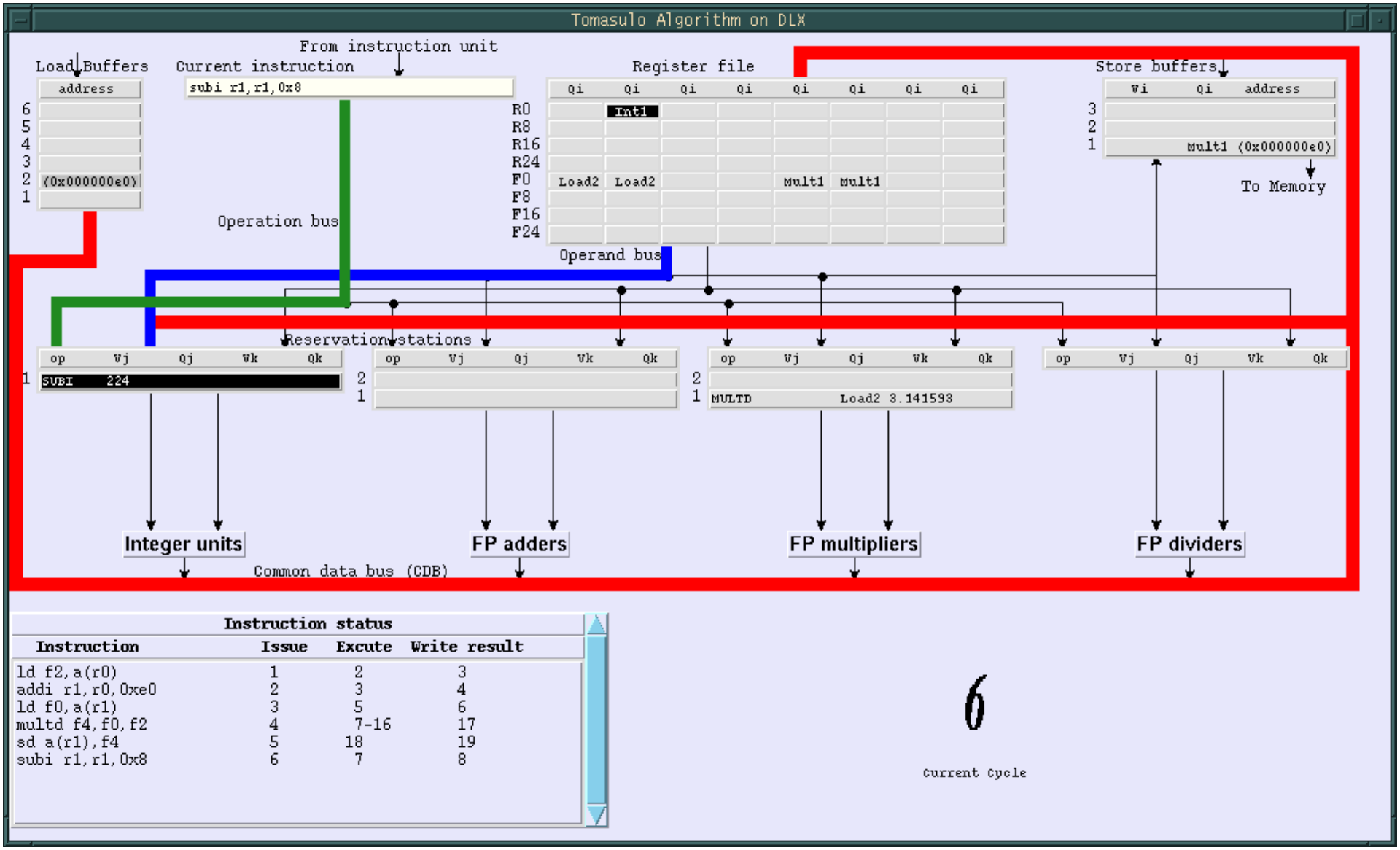

Tomasulo Algorithm on DLX
From instruction unit
Load Buffers
Current instruction
ld f2,a(r0)
Register file
Store buffers
address
Qi
Vi
Load1
To Memory
Operation bus
Operand bus
Reservation stations
op
Vj
Qj
Vk
Qk
Integer units
FP adders
FP multipliers
FP dividers
Common data bus (CDB)
Instruction status
Instruction
Issue
Excute
Write result
ld f2,a(r0)
1
2
3
Current Cycle

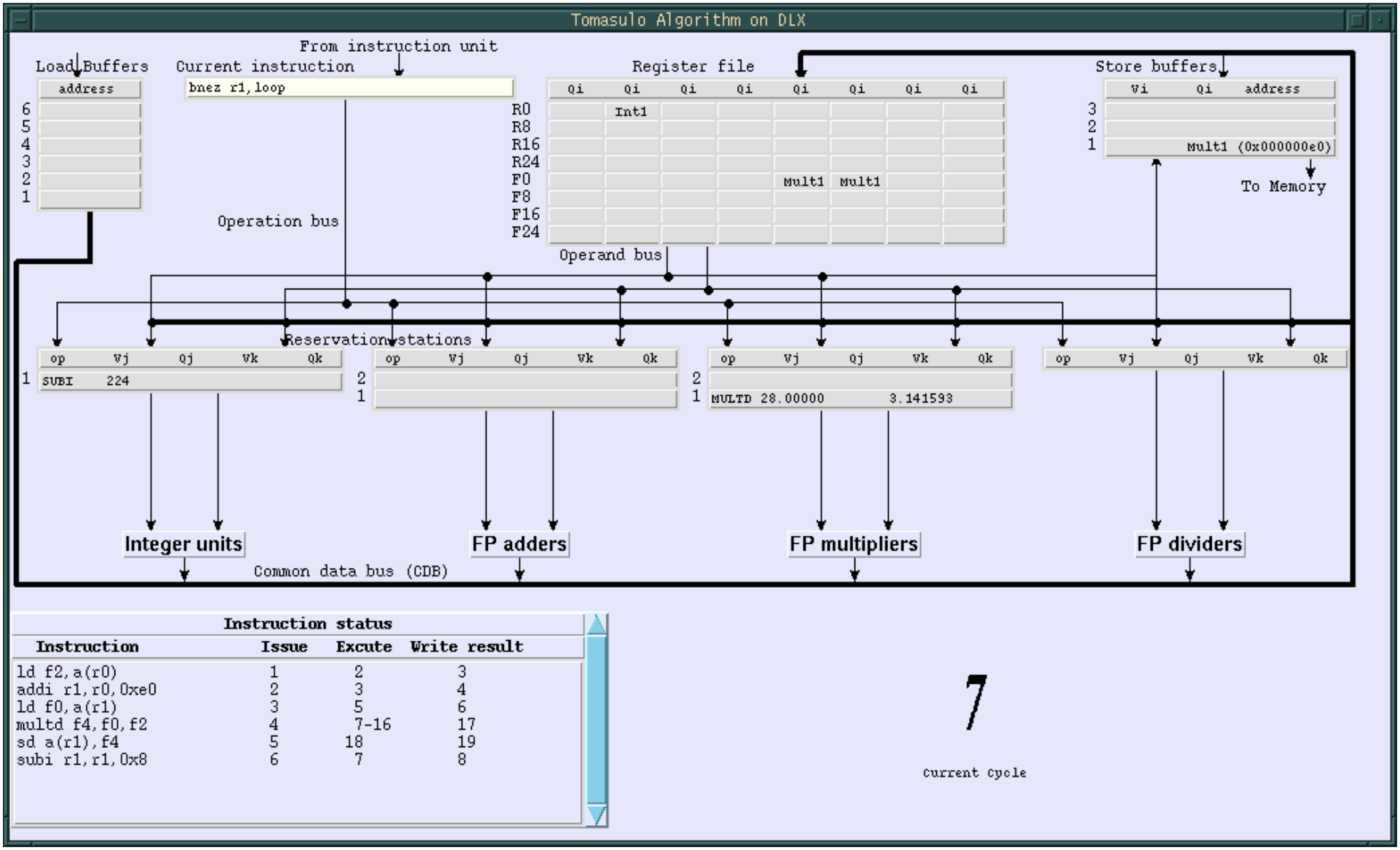

Tomasulo Algorithm on DLX
From instruction unit
Load Buffers
Current instruction
addi r1,r0,0xe0
address
(0x00000000)
Register file
Qi
R0
R8
R16
R24
F0
F8
F16
F24
Int1
Load1
Load1
Store buffers
Vi
Qi
address
To Memory
Operation bus
Operand bus
Reservation stations
op
Vj
Qj
Vk
Qk
ADDI
0
Integer units
FP adders
FP multipliers
FP dividers
Common data bus (CDB)
Instruction status
Instruction
Issue
Excute
Write result
ld f2,a(r0)
addi r1,r0,0xe0
2
Current Cycle


Tomasulo Algorithm on DLX
From instruction unit
Load Buffers
Current instruction
ld f0,a(r1)
Register file
Store buffers
address
Qi
Vi
Int1
Load2
Load1
(0x000000e0)
(0x00000000)
Operation bus
Operand bus
To Memory
Reservation stations
op
Vj
Qj
Vk
Qk
ADDI
Integer units
FP adders
FP multipliers
FP dividers
Common data bus (CDB)
Instruction status
Instruction
Issue
Excute
Write result
ld f2,a(r0) 1 2 3
addi r1,r0,0xe0 2 3 4
ld f0,a(r1) 3 5 6
3
Current Cycle


Tomasulo Algorithm on DLX
From instruction unit
Load Buffers
Current instruction
multd f4,f0,f2
address
6
5
4
3
2 (0x000000e0)
1
Register file
Qi Qi Qi Qi Qi Qi Qi Qi
R0 Int1
R8
R16
R24
F0 Load2 Load2 Mult1 Mult1
F8
F16
F24
Store buffers
Vi Qi address
3
2
1
To Memory
Operation bus
Operand bus
Reservation stations
op Vj Qj Vk Qk
1 ADDI 0
2
1
2
1 MULTD Load2 3.141593
Integer units
FP adders
FP multipliers
FP dividers
Common data bus (CDB)
Instruction status
Instruction Issue Excute Write result
ld f2,a(r0) 1 2 3
addi r1,r0,0xe0 2 3 4
ld f0,a(r1) 3 5 6
multd f4,f0,f2 4 7-16 17
4
Current Cycle


Tomasulo Algorithm on DLX
From instruction unit
Load Buffers
Current instruction
address
sd a(r1),f4
6
5
4
3
2 (0x000000e0)
1
Operation bus
Register file
Qi Qi Qi Qi Qi Qi Qi Qi
R0
R8
R16
R24
F0 Load2 Load2 Mult1 Mult1
F8
F16
F24
Operand bus
Store buffers
Vi Qi address
3
2
1 Mult1 (0x000000e0)
To Memory
Reservation stations
op Vj Qj Vk Qk
1
2
1
2
1 MULTD Load2 3.141593
Integer units
FP adders
FP multipliers
FP dividers
Common data bus (CDB)
Instruction status
Instruction Issue Excute Write result
ld f2,a(r0) 1 2 3
addi r1,r0,0xe0 2 3 4
ld f0,a(r1) 3 5 6
multd f4,f0,f2 4 7-16 17
sd a(r1),f4 5 18 19
5
Current Cycle


Tomasulo Algorithm on DLX
From instruction unit
Load Buffers
address
Current instruction
subi r1,r1,0x8
Register file
Qi Qi Qi Qi Qi Qi Qi Qi
R0 Int1
R8
R16
R24
F0 Load2 Load2 Mult1 Mult1
F8
F16
F24
Store buffers
Vi Qi address
3
2
1 Mult1 (0x000000e0)
To Memory
6
5
4
3
2 (0x000000e0)
1
Operation bus
Operand bus
Reservation stations
op Vj Qj Vk Qk
1 SUBI 224
2
1
2
1 MULTD Load2 3.141593
Integer units
FP adders
FP multipliers
FP dividers
Common data bus (CDB)
Instruction status
Instruction Issue Excute Write result
ld f2,a(r0) 1 2 3
addi r1,r0,0xe0 2 3 4
ld f0,a(r1) 3 5 6
multd f4,f0,f2 4 7-16 17
sd a(r1),f4 5 18 19
subi r1,r1,0x8 6 7 8
6
Current Cycle

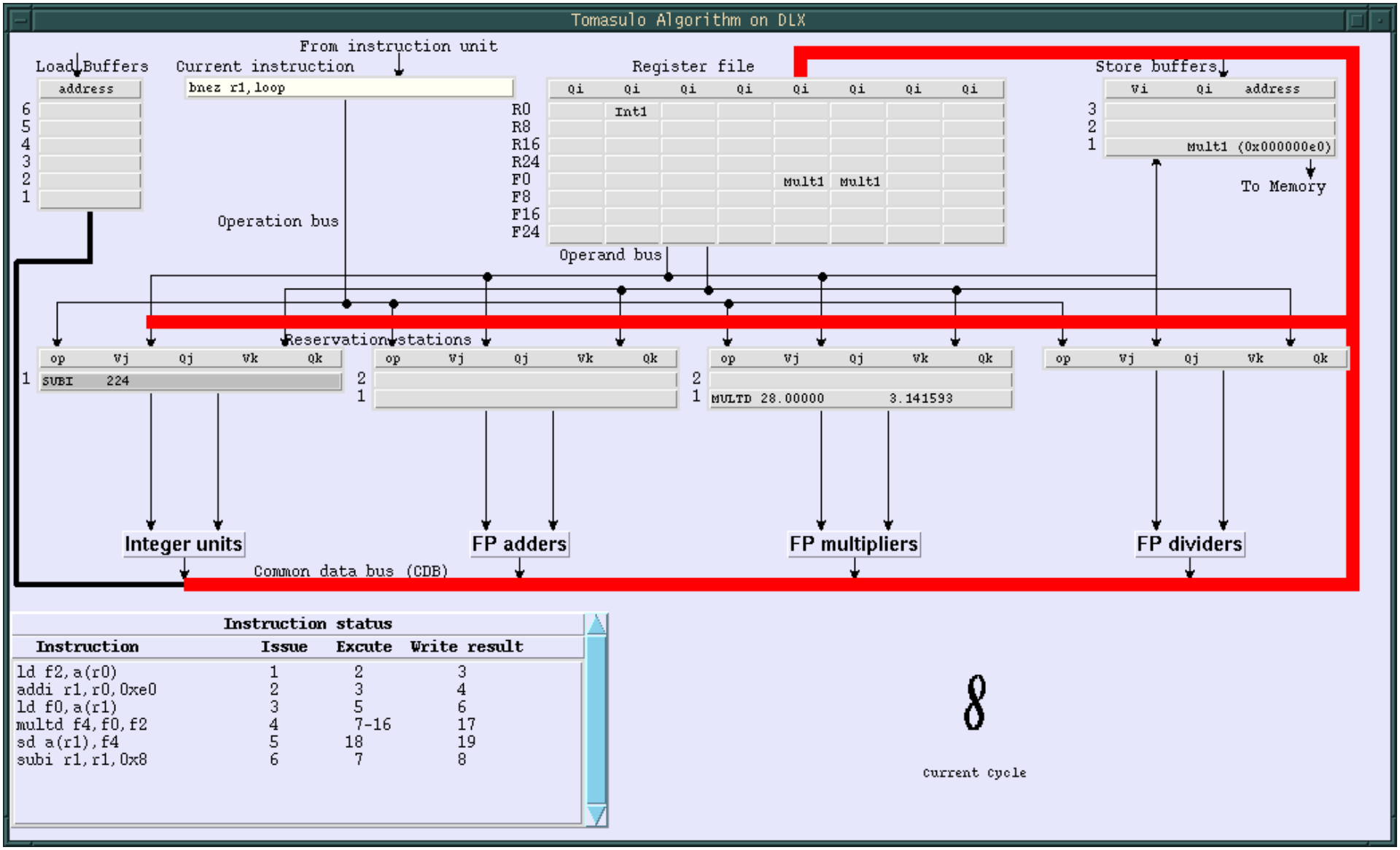


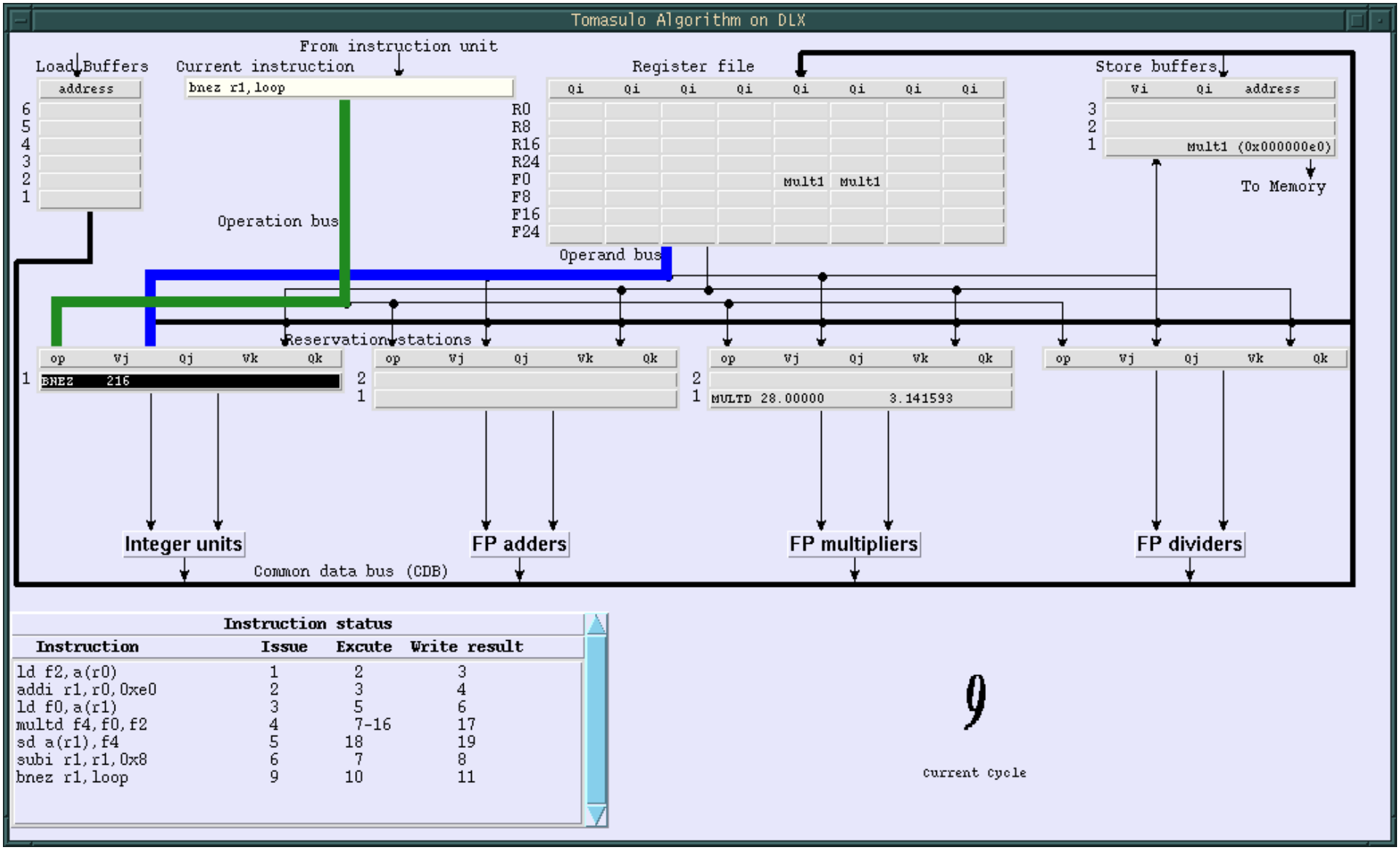
Instruction status

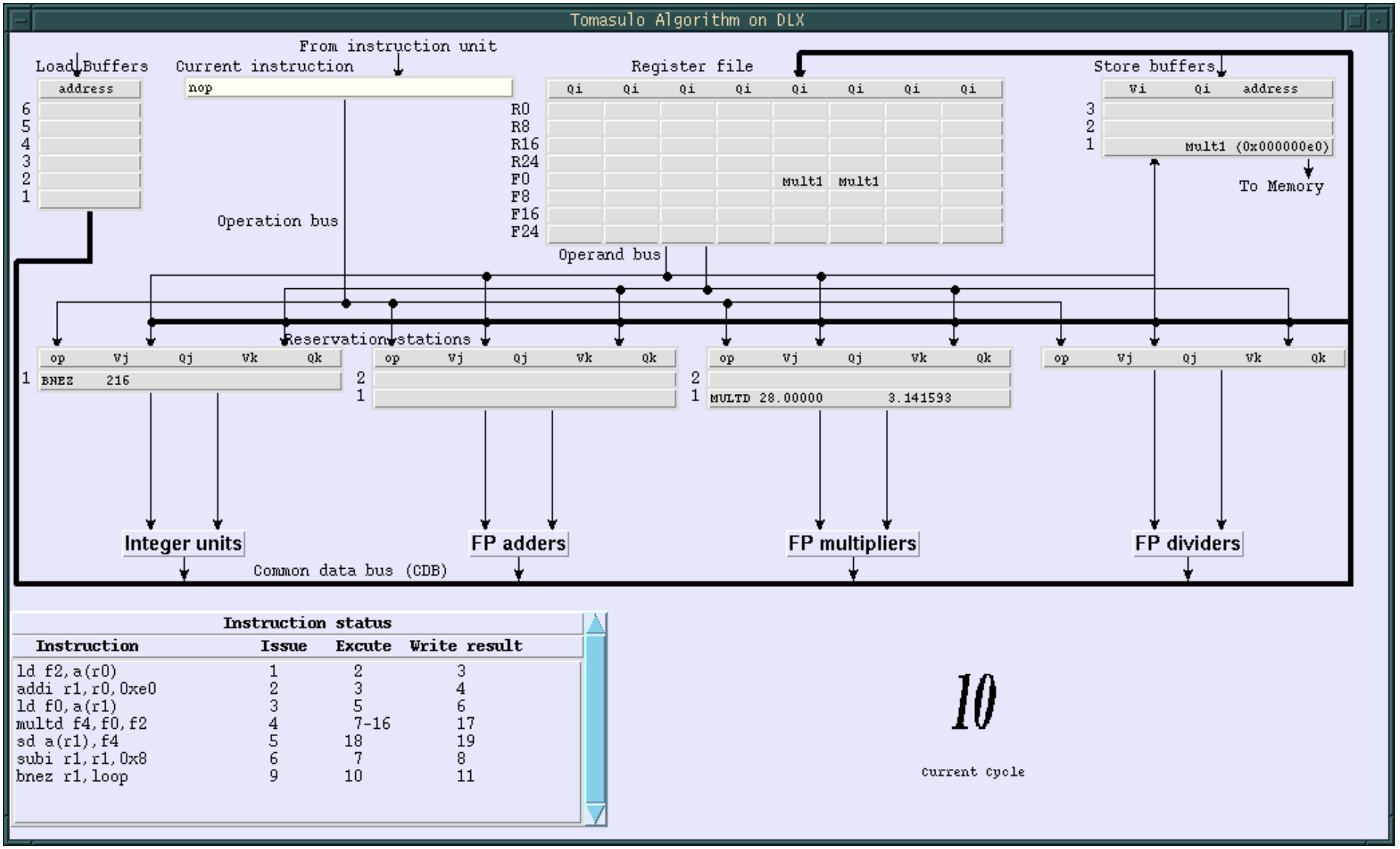
Instruction	Issue	Excute	Write result
ld f2,a(r0)	1	2	3
addi r1,r0,0xe0	2	3	4
ld f0,a(r1)	3	5	6
multd f4,f0,f2	4	7-16	17
sd a(r1),f4	5	18	19
subi r1,r1,0x8	6	7	8

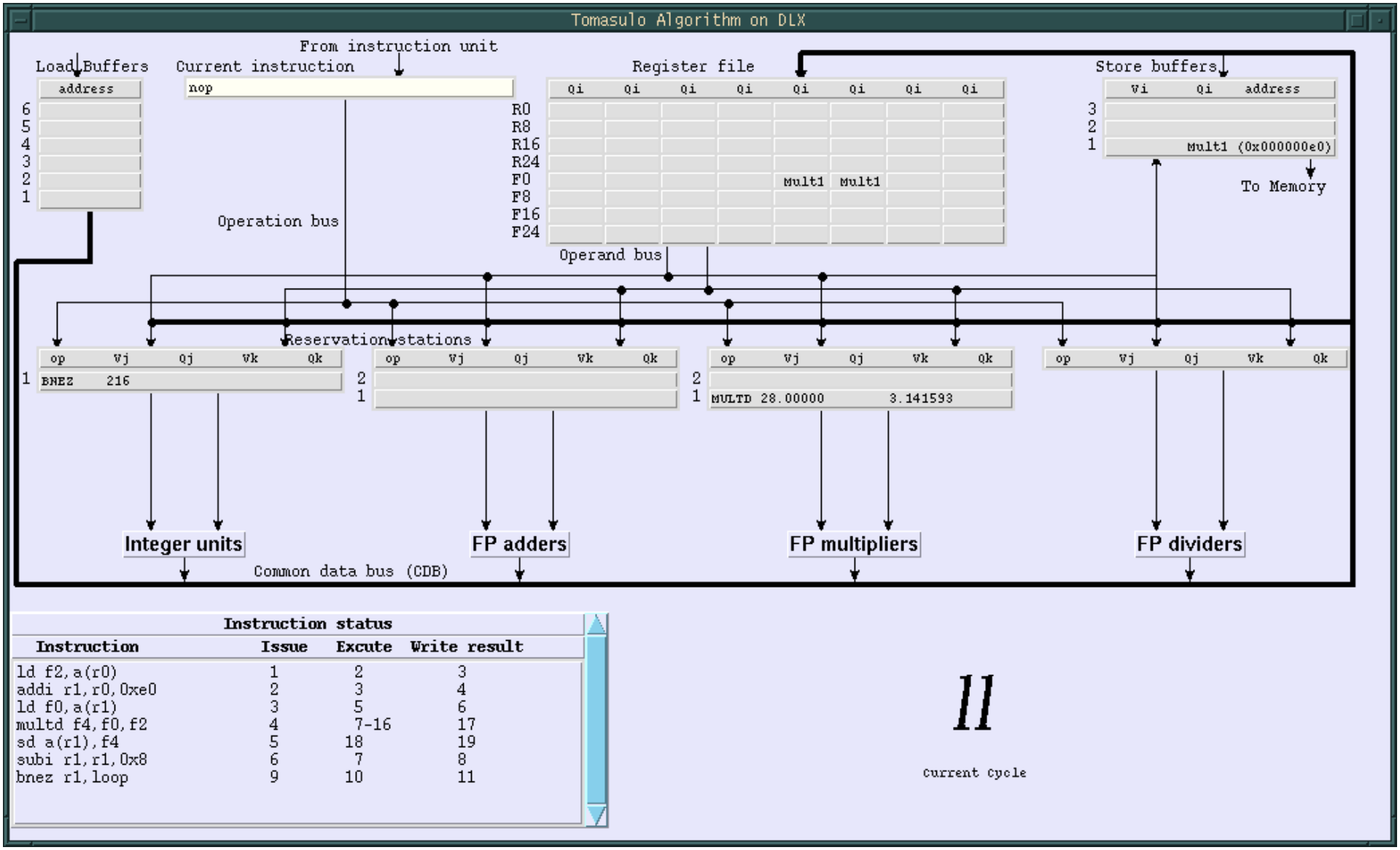
7

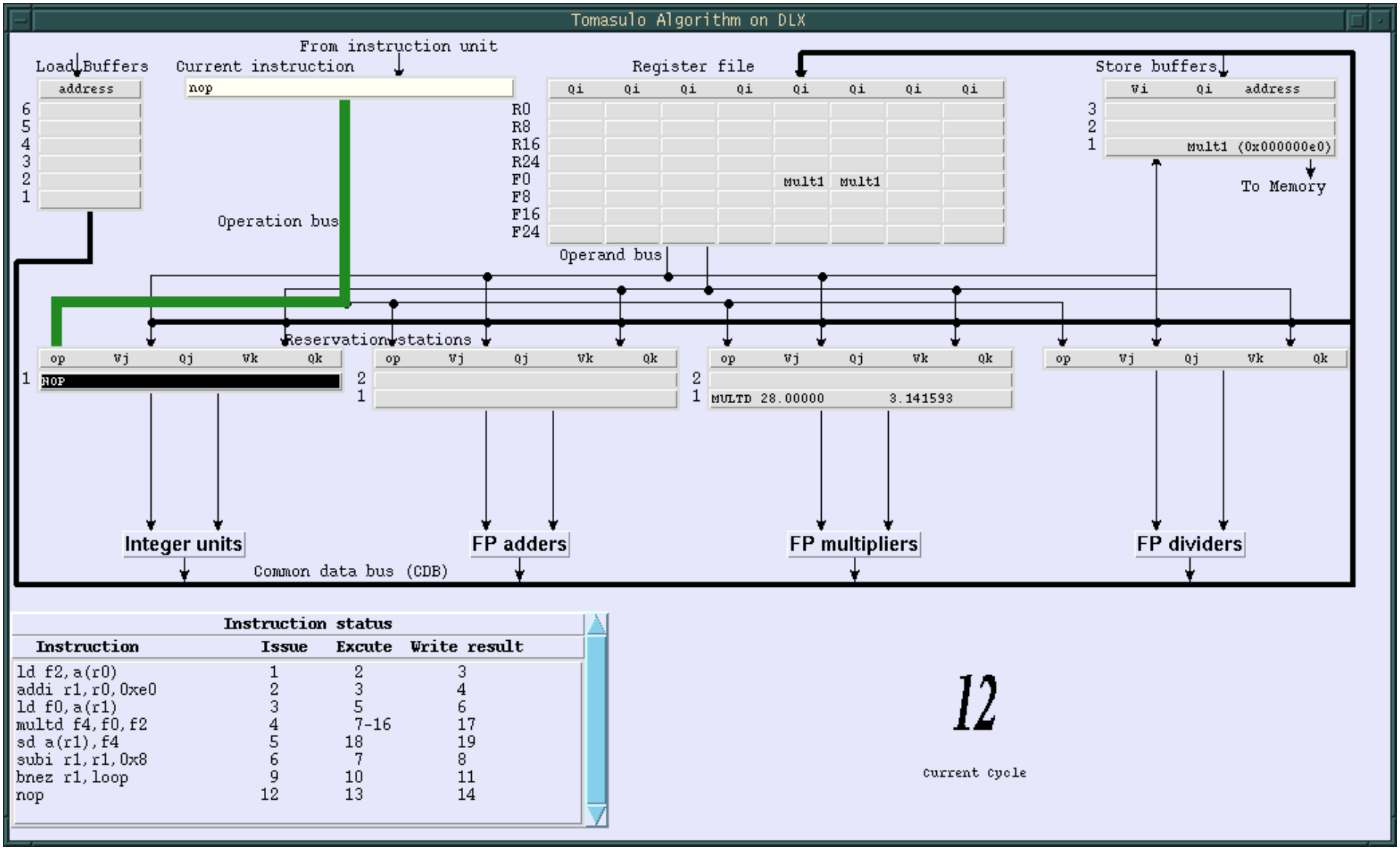
Current Cycle

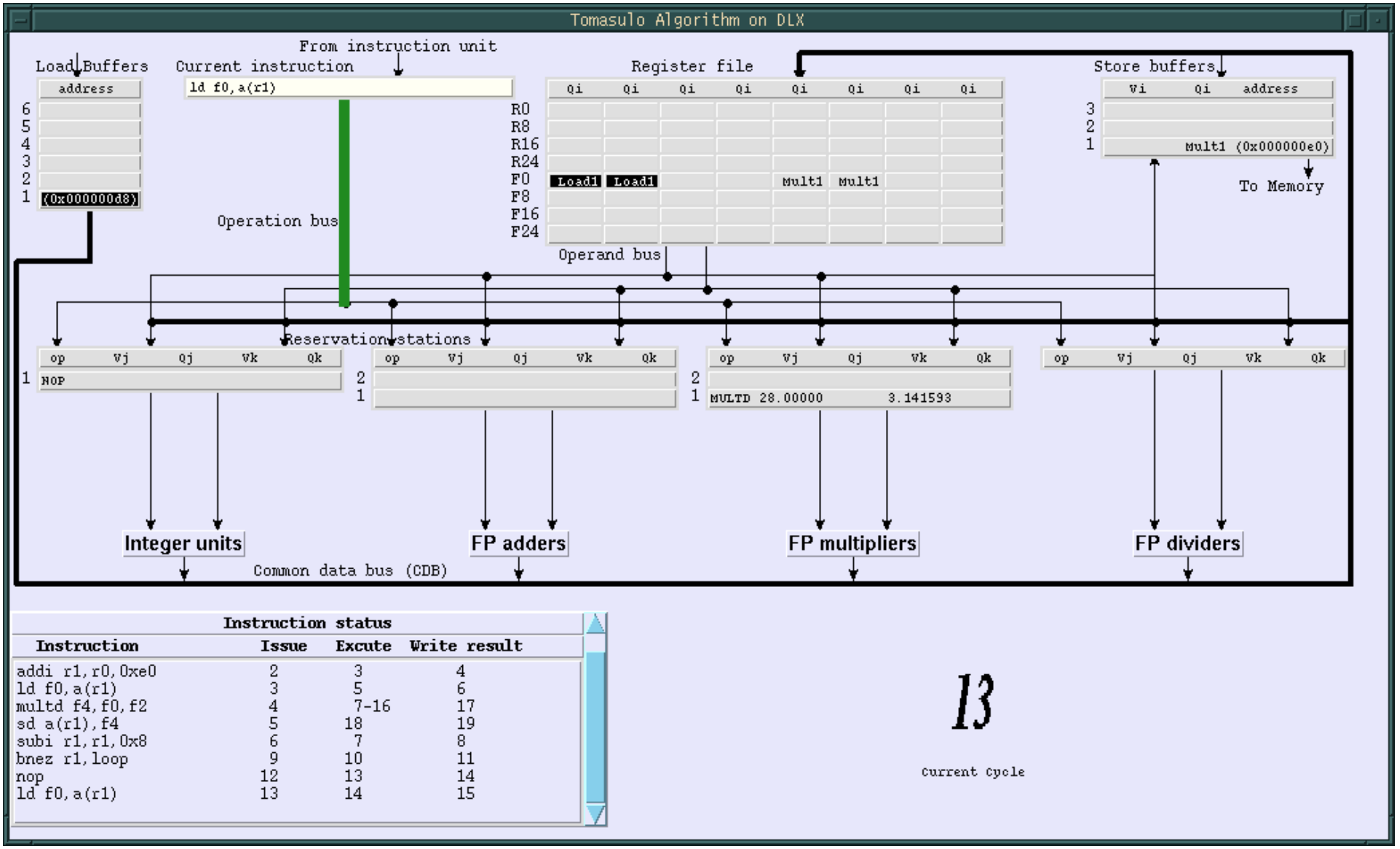

Tomasulo Algorithm on DLX
From instruction unit
Load Buffers
Current instruction
bnez r1,loop
address
Register file
Qi
R0
R8
R16
R24
F0
F8
F16
F24
Int1
Mult1
Mult1
Store buffers
Vi
Qi
address
Mult1 (0x000000e0)
To Memory
Operation bus
Operand bus
Reservation stations
op
Vj
Qj
Vk
Qk
SUBI
224
MULTD
28.00000
3.141593
Integer units
FP adders
FP multipliers
FP dividers
Common data bus (CDB)
Instruction status
Instruction
Issue
Excute
Write result
ld f2,a(r0) 1 2 3
addi r1,r0,0xe0 2 3 4
ld f0,a(r1) 3 5 6
multd f4,f0,f2 4 7-16 17
sd a(r1),f4 5 18 19
subi r1,r1,0x8 6 7 8
8
Current Cycle

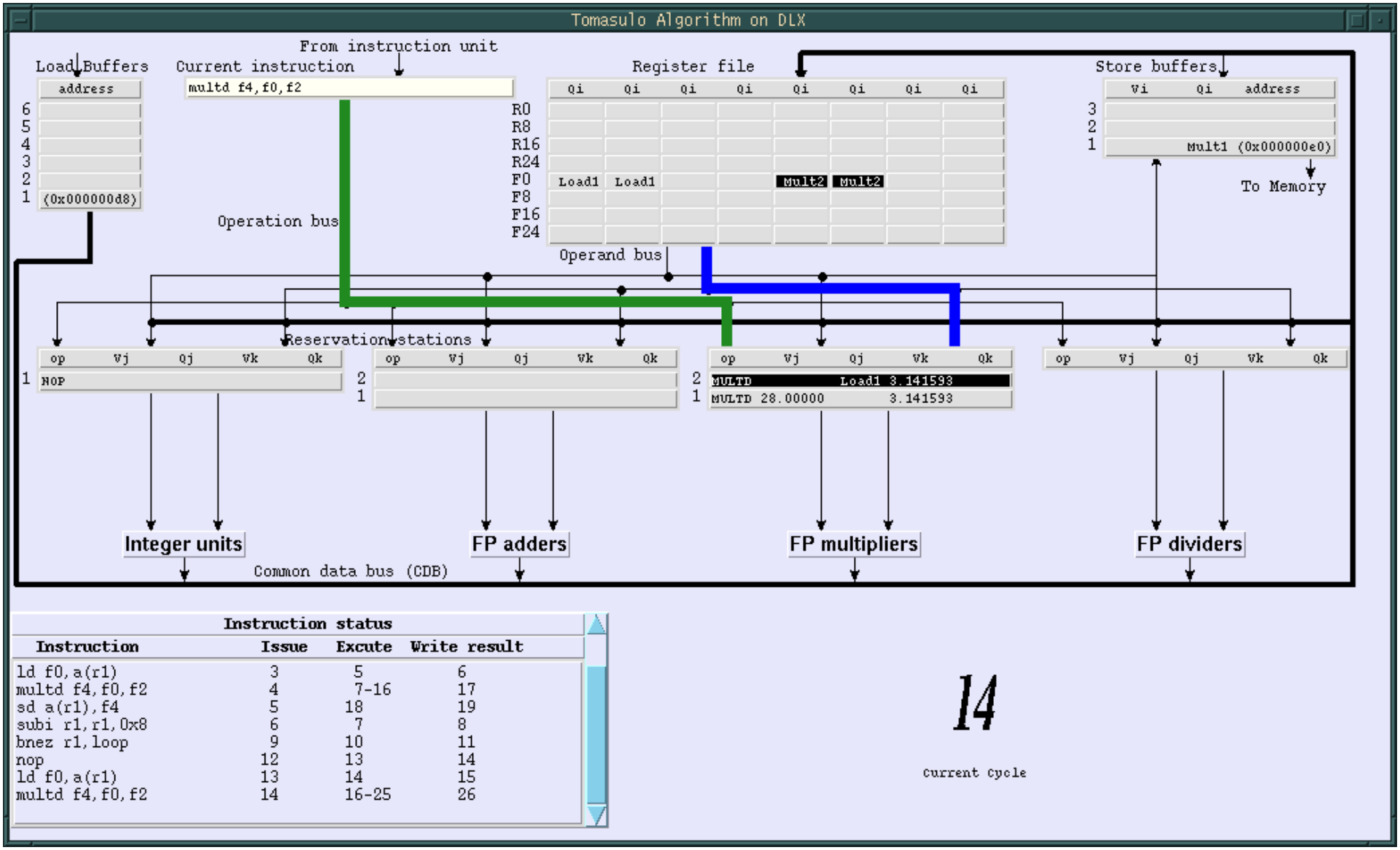

Tomasulo Algorithm on DLX
From instruction unit
Load Buffers
Current instruction
address
bnez r1,loop
Register file
Qi
R0
R8
R16
R24
F0
F8
F16
F24
Mult1
Store buffers
Vi
address
Mult1 (0x000000e0)
To Memory
Operation bus
Operand bus
Reservation stations
op
Vj
Qj
Vk
Qk
BNEZ 216
MULTD 28.00000 3.141593
Integer units
FP adders
FP multipliers
FP dividers
Common data bus (CDB)
Instruction status
Instruction
Issue
Excute
Write result
ld f2,a(r0) 1 2 3
addi r1,r0,0xe0 2 3 4
ld f0,a(r1) 3 5 6
multd f4,f0,f2 4 7-16 17
sd a(r1),f4 5 18 19
subi r1,r1,0x8 6 7 8
bnez r1,loop 9 10 11
9
Current Cycle


Tomasulo Algorithm on DLX
From instruction unit
Load Buffers
Current instruction
nop
address
Register file
Qi
Store buffers
Vi
Qi
address
Mult1 (0x000000e0)
To Memory
Operation bus
Operand bus
Mult1
Reservation stations
op
Vj
Qj
Vk
Qk
BNEZ
216
MULTD
28.00000
3.141593
Integer units
FP adders
FP multipliers
FP dividers
Common data bus (CDB)
Instruction status
Instruction
Issue
Excute
Write result
ld f2,a(r0) 1 2 3
addi r1,r0,0xe0 2 3 4
ld f0,a(r1) 3 5 6
multd f4,f0,f2 4 7-16 17
sd a(r1),f4 5 18 19
subi r1,r1,0x8 6 7 8
bnez r1,loop 9 10 11
10
Current Cycle


Tomasulo Algorithm on DLX
From instruction unit
Load Buffers
Current instruction
nop
address
Register file
Qi
Store buffers
Vi
Qi
address
Mult1 (0x000000e0)
To Memory
Operation bus
Operand bus
Mult1
Reservation stations
op
Vj
Qj
Vk
Qk
BNEZ
216
MULTD
28.00000
3.141593
Integer units
FP adders
FP multipliers
FP dividers
Common data bus (CDB)
Instruction status
Instruction
Issue
Excute
Write result
ld f2,a(r0) 1 2 3
addi r1,r0,0xe0 2 3 4
ld f0,a(r1) 3 5 6
multd f4,f0,f2 4 7-16 17
sd a(r1),f4 5 18 19
subi r1,r1,0x8 6 7 8
bnez r1,loop 9 10 11
11
Current Cycle


Tomasulo Algorithm on DLX
From instruction unit
Load Buffers
Current instruction
nop
address
Register file
Qi
R0
R8
R16
R24
F0
F8
F16
F24
Mult1
Store buffers
Vi
Mult1 (0x000000e0)
To Memory
Operation bus
Operand bus
Reservation stations
op
Vj
Qj
Vk
Qk
NOP
MULTD 28.00000
3.141593
Integer units
FP adders
FP multipliers
FP dividers
Common data bus (CDB)
Instruction status
Instruction
Issue
Excute
Write result
ld f2,a(r0) 1 2 3
addi r1,r0,0xe0 2 3 4
ld f0,a(r1) 3 5 6
multd f4,f0,f2 4 7-16 17
sd a(r1),f4 5 18 19
subi r1,r1,0x8 6 7 8
bnez r1,loop 9 10 11
nop 12 13 14
12
Current Cycle


Tomasulo Algorithm on DLX
From instruction unit
Load Buffers
Current instruction
ld f0,a(r1)
Register file
Store buffers
address
Qi
Vi
Operation bus
Operand bus
To Memory
Mult1 (0x000000e0)
(0x000000d8)
Load1
Mult1
Reservation stations
op
Vj
Qj
Vk
Qk
NOP
MULTD 28.00000
3.141593
Integer units
FP adders
FP multipliers
FP dividers
Common data bus (CDB)
Instruction status
Instruction
Issue
Excute
Write result
addi r1,r0,0xe0 2 3 4
ld f0,a(r1) 3 5 6
multd f4,f0,f2 4 7-16 17
sd a(r1),f4 5 18 19
subi r1,r1,0x8 6 7 8
bnez r1,loop 9 10 11
nop 12 13 14
ld f0,a(r1) 13 14 15
13
Current Cycle

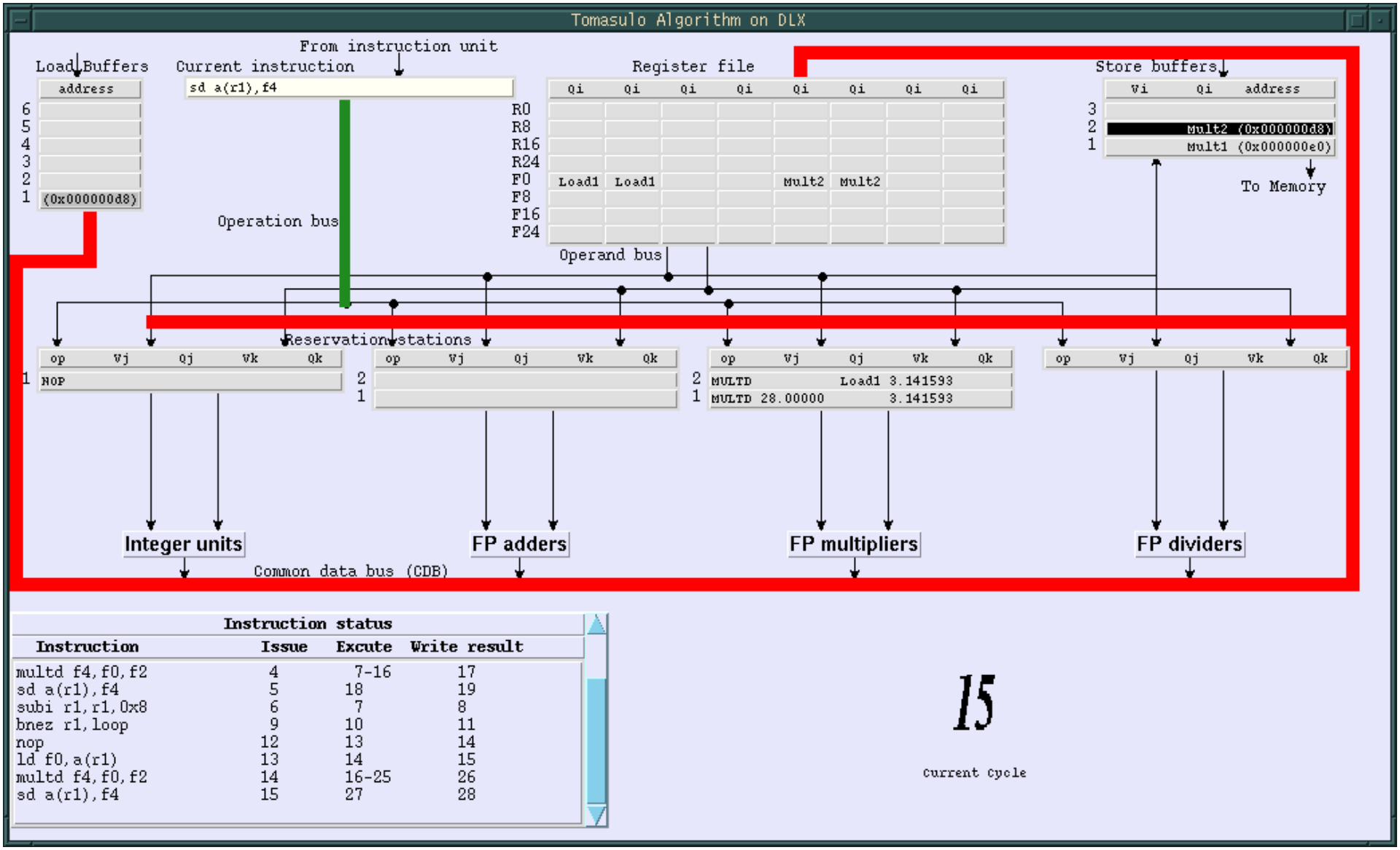


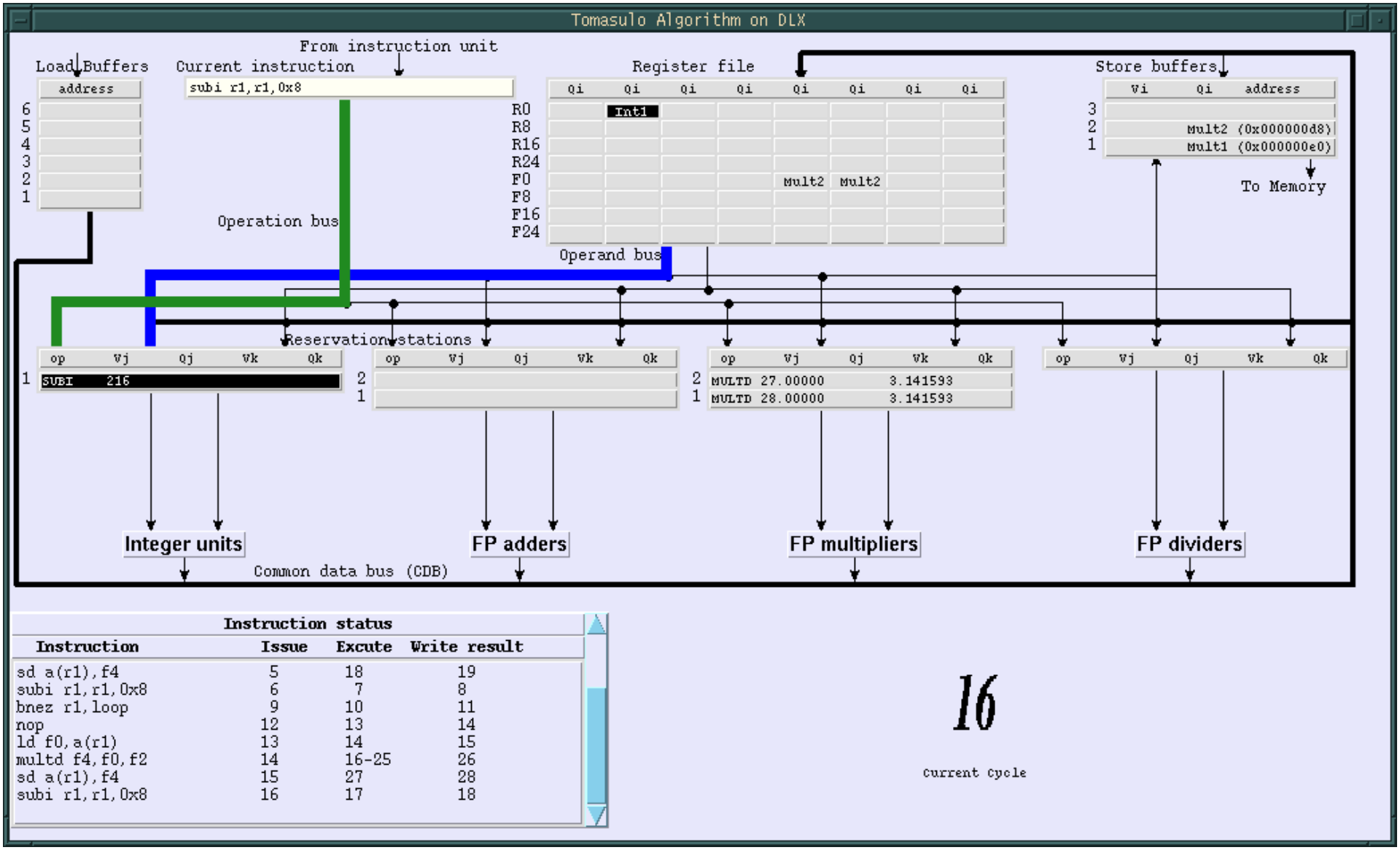
Instruction status

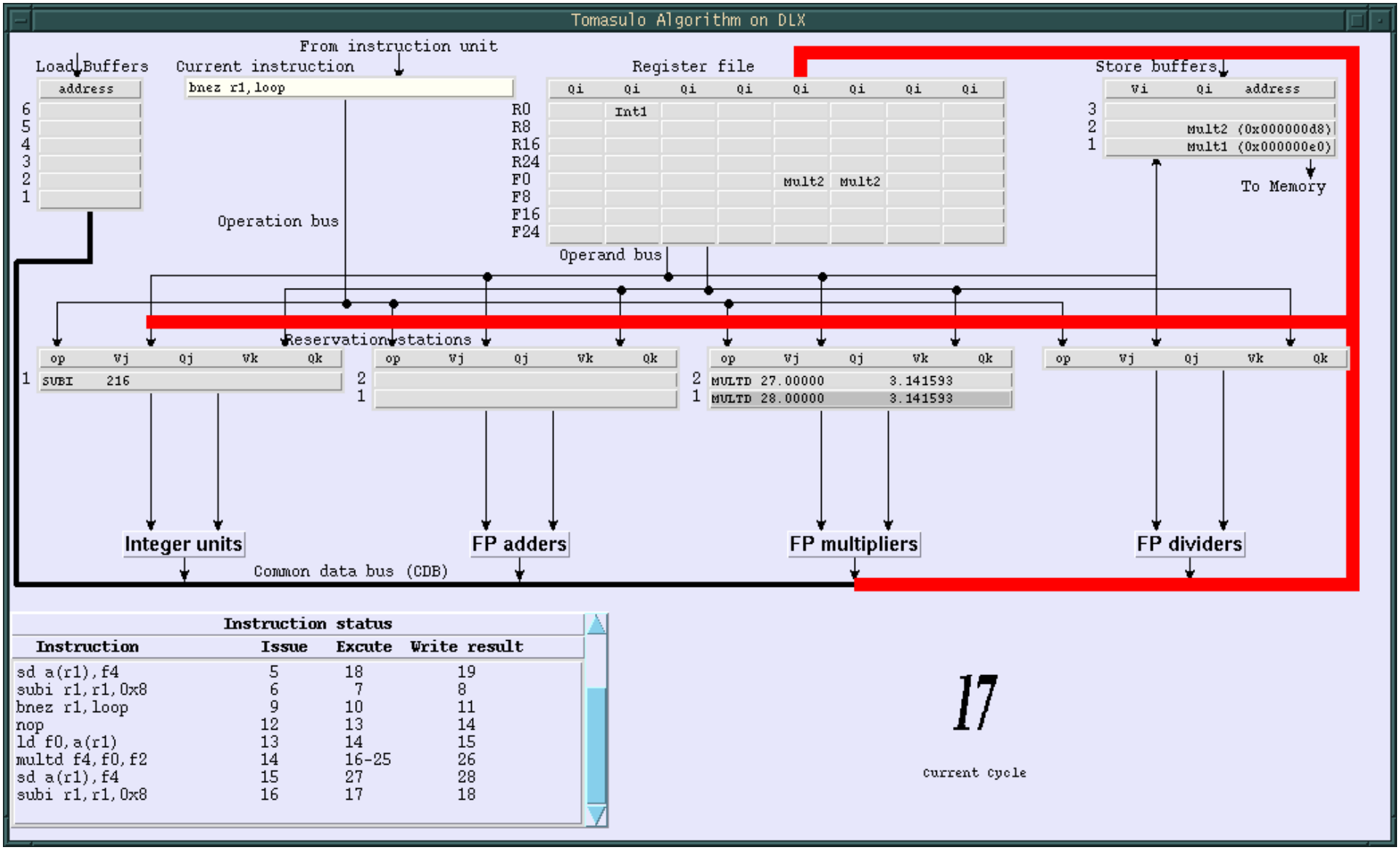
Instruction	Issue	Excute	Write result
ld f0,a(r1)	3	5	6
multd f4,f0,f2	4	7-16	17
sd a(r1),f4	5	18	19
subi r1,r1,0x8	6	7	8
bnez r1,loop	9	10	11
nop	12	13	14
ld f0,a(r1)	13	14	15
multd f4,f0,f2	14	16-25	26

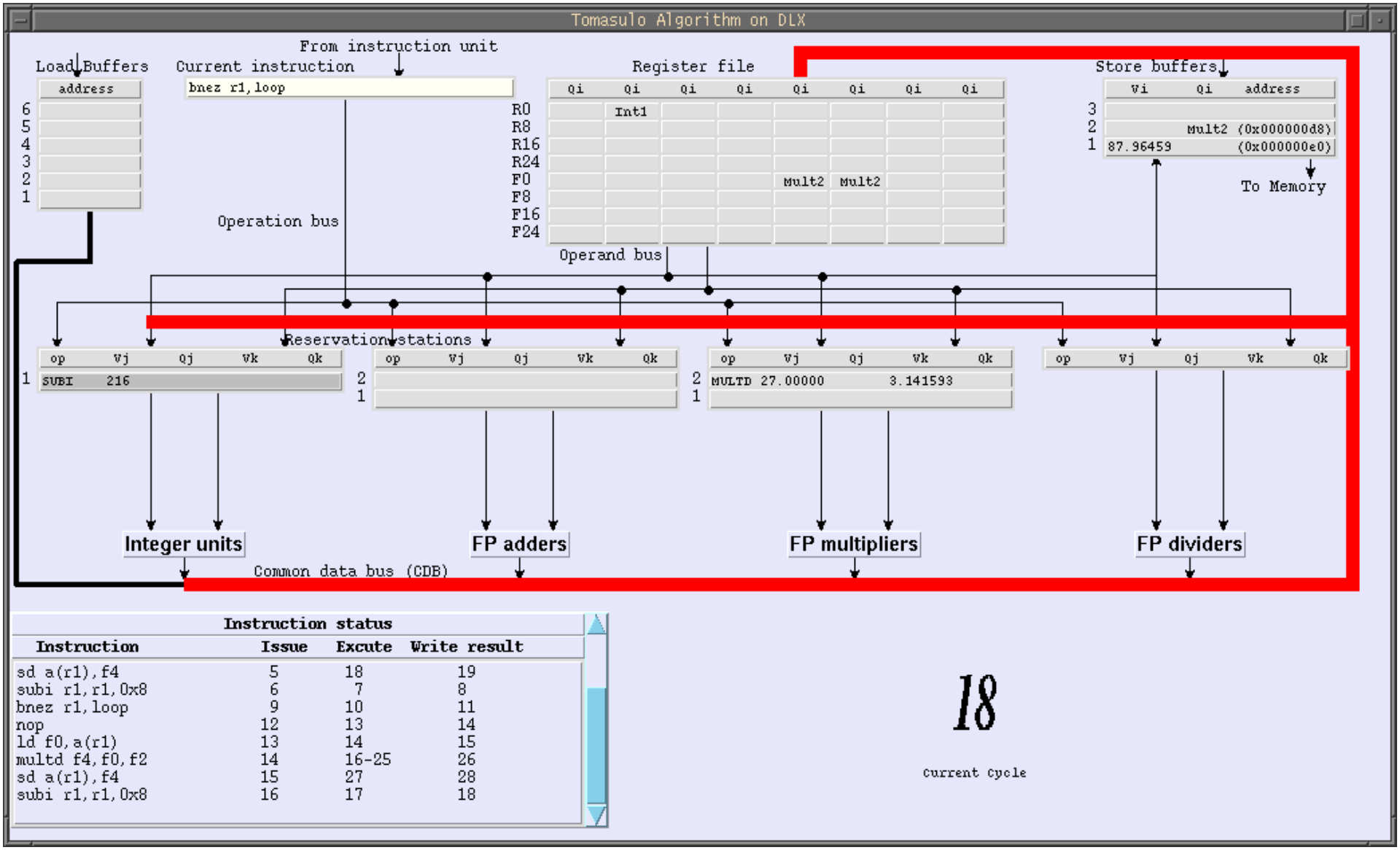
14

Current Cycle


Tomasulo Algorithm on DLX
From instruction unit
Load Buffers
Current instruction
address
sd a(r1),f4
6
5
4
3
2
1
(0x000000d8)
Operation bus
Register file
Qi Qi Qi Qi Qi Qi Qi Qi
R0
R8
R16
R24
F0 Load1 Load1 Mult2 Mult2
F8
F16
F24
Operand bus
Store buffers
Vi Qi address
3
2 Mult2 (0x000000d8)
1 Mult1 (0x000000e0)
To Memory
Reservation stations
op Vj Qj Vk Qk
1 NOP
2
1
2 MULTD Load1 3.141593
1 MULTD 28.00000 3.141593
Integer units
FP adders
FP multipliers
FP dividers
Common data bus (CDB)
Instruction status
Instruction Issue Excute Write result
multd f4,f0,f2 4 7-16 17
sd a(r1),f4 5 18 19
subi r1,r1,0x8 6 7 8
bnez r1,loop 9 10 11
nop 12 13 14
ld f0,a(r1) 13 14 15
multd f4,f0,f2 14 16-25 26
sd a(r1),f4 15 27 28
15
Current Cycle


Tomasulo Algorithm on DLX
From instruction unit
Load Buffers
Current instruction
address
subi r1,r1,0x8
Register file
Qi
Int1
R0
R8
R16
R24
F0
F8
F16
F24
Mult2
Store buffers
Vi
Qi
address
Mult2 (0x000000d8)
Mult1 (0x000000e0)
To Memory
Operation bus
Operand bus
Reservation stations
op
Vj
Qj
Vk
Qk
SUBI
216
MULTD 27.00000
3.141593
MULTD 28.00000
3.141593
Integer units
FP adders
FP multipliers
FP dividers
Common data bus (CDB)
Instruction status
Instruction
Issue
Excute
Write result
sd a(r1),f4 5 18 19
subi r1,r1,0x8 6 7 8
bnez r1,loop 9 10 11
nop 12 13 14
ld f0,a(r1) 13 14 15
multd f4,f0,f2 14 16-25 26
sd a(r1),f4 15 27 28
subi r1,r1,0x8 16 17 18
16
Current Cycle


Tomasulo Algorithm on DLX
From instruction unit
Load Buffers
address
Current instruction
bnez r1,loop
Register file
Qi
R0
R8
R16
R24
F0
F8
F16
F24
Int1
Mult2
Store buffers
Vi
address
Mult2 (0x000000d8)
Mult1 (0x000000e0)
To Memory
Operation bus
Operand bus
Reservation stations
op
Vj
Qj
Vk
Qk
SUBI 216
MULTD 27.00000 3.141593
MULTD 28.00000 3.141593
Integer units
FP adders
FP multipliers
FP dividers
Common data bus (CDB)
Instruction status
Instruction
Issue
Excute
Write result
sd a(r1),f4 5 18 19
subi r1,r1,0x8 6 7 8
bnez r1,loop 9 10 11
nop 12 13 14
ld f0,a(r1) 13 14 15
multd f4,f0,f2 14 16-25 26
sd a(r1),f4 15 27 28
subi r1,r1,0x8 16 17 18
17
Current Cycle


Tomasulo Algorithm on DLX
From instruction unit
Load Buffers
address
Current instruction
bnez r1,loop
Register file
Qi
R0
R8
R16
R24
F0
F8
F16
F24
Int1
Mult2
Store buffers
Vi
address
Mult2 (0x000000d8)
87.96459
(0x000000e0)
To Memory
Operation bus
Operand bus
Reservation stations
op
Vj
Qj
Vk
Qk
SUBI 216
MULTD 27.00000 3.141593
Integer units
FP adders
FP multipliers
FP dividers
Common data bus (CDB)
Instruction status
Instruction
Issue
Excute
Write result
sd a(r1),f4 5 18 19
subi r1,r1,0x8 6 7 8
bnez r1,loop 9 10 11
nop 12 13 14
ld f0,a(r1) 13 14 15
multd f4,f0,f2 14 16-25 26
sd a(r1),f4 15 27 28
subi r1,r1,0x8 16 17 18
18
Current Cycle