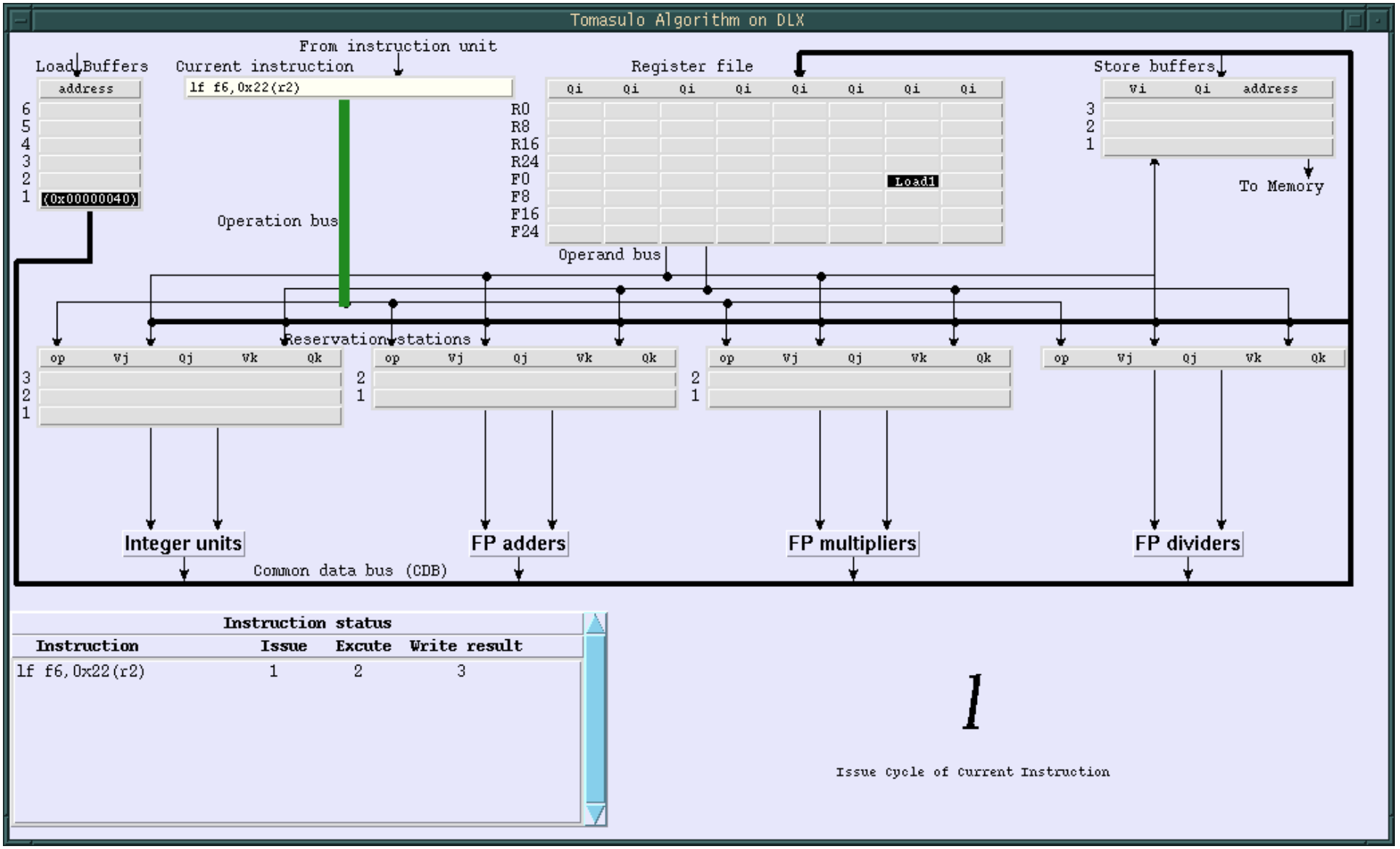
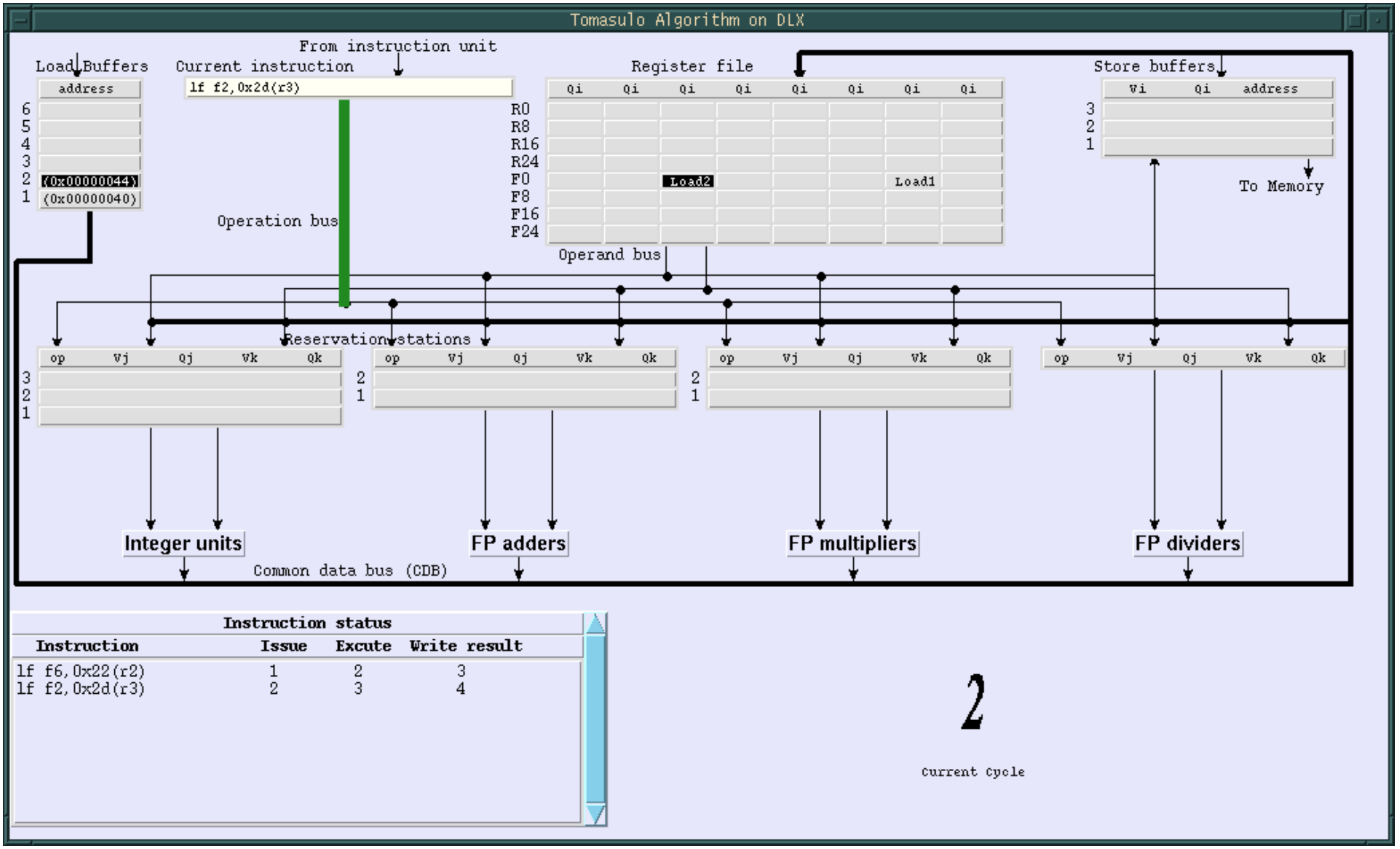
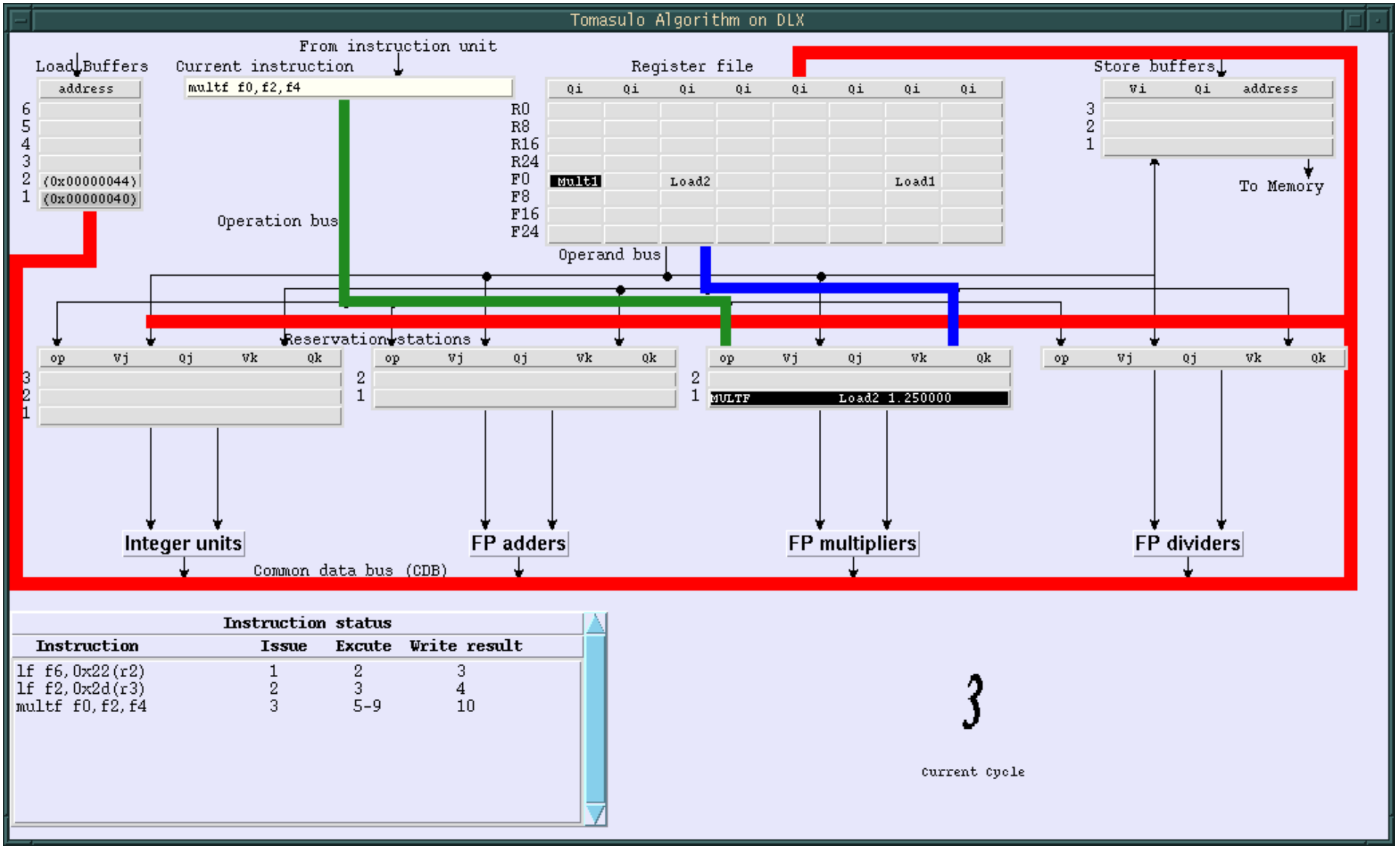
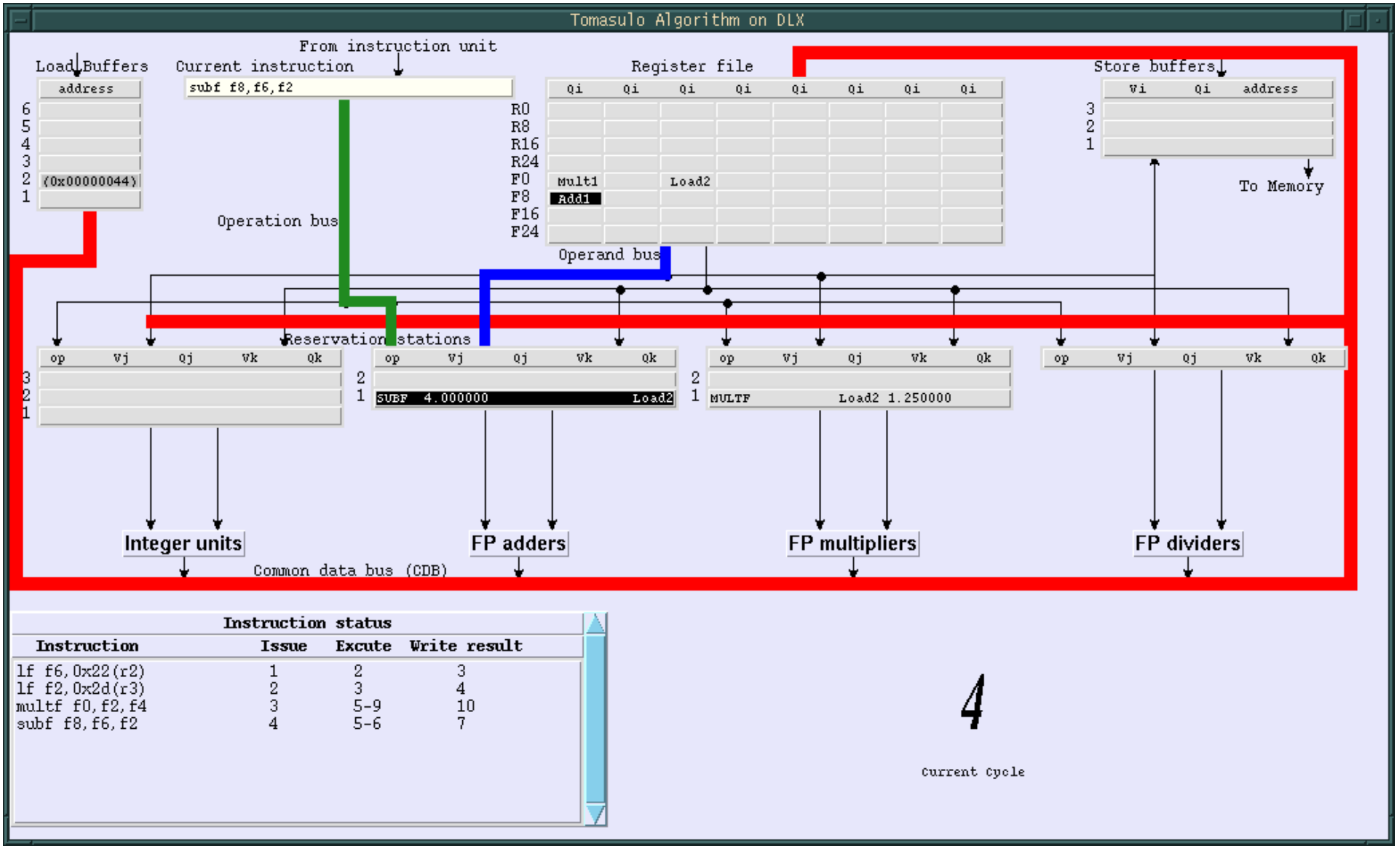
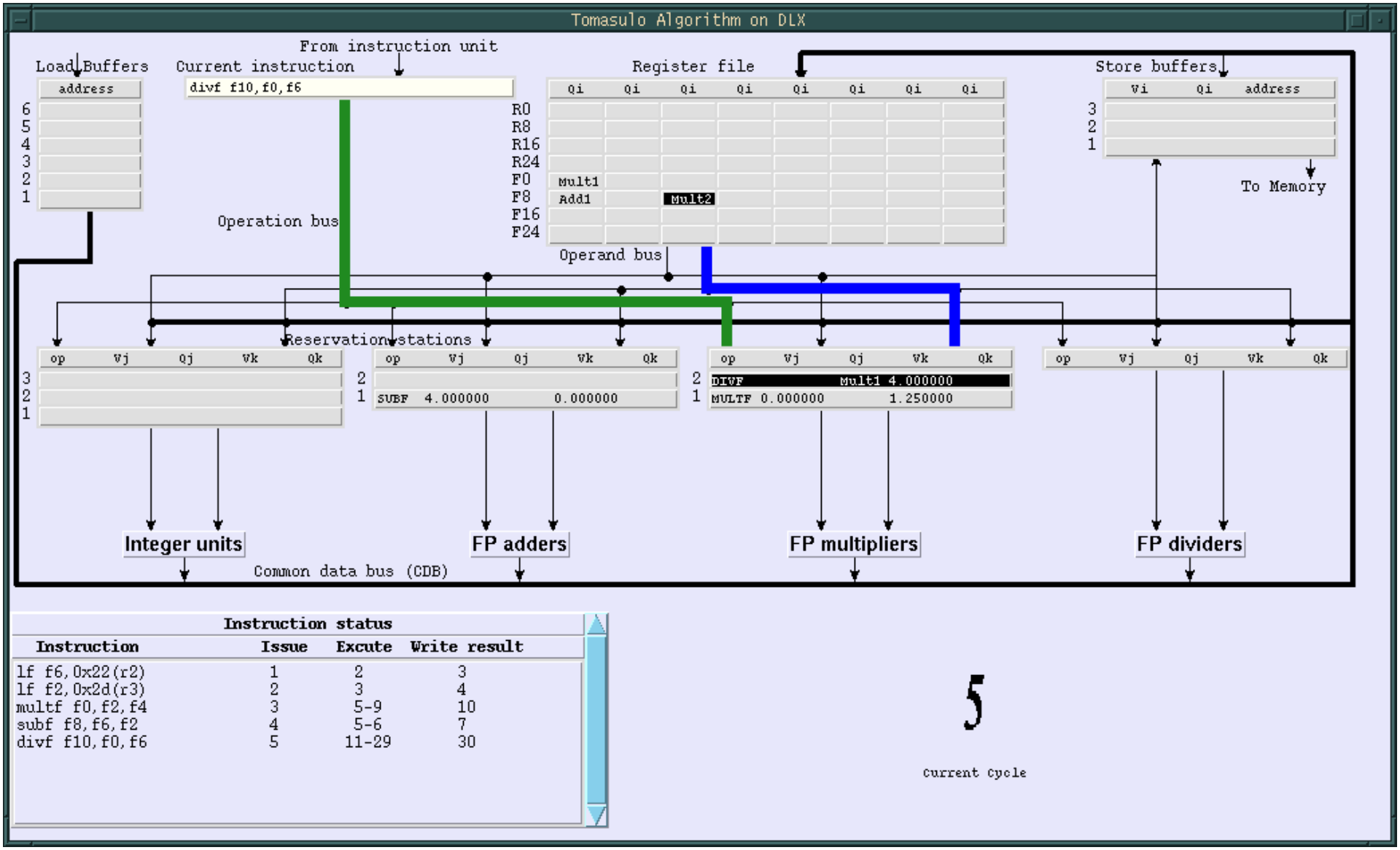
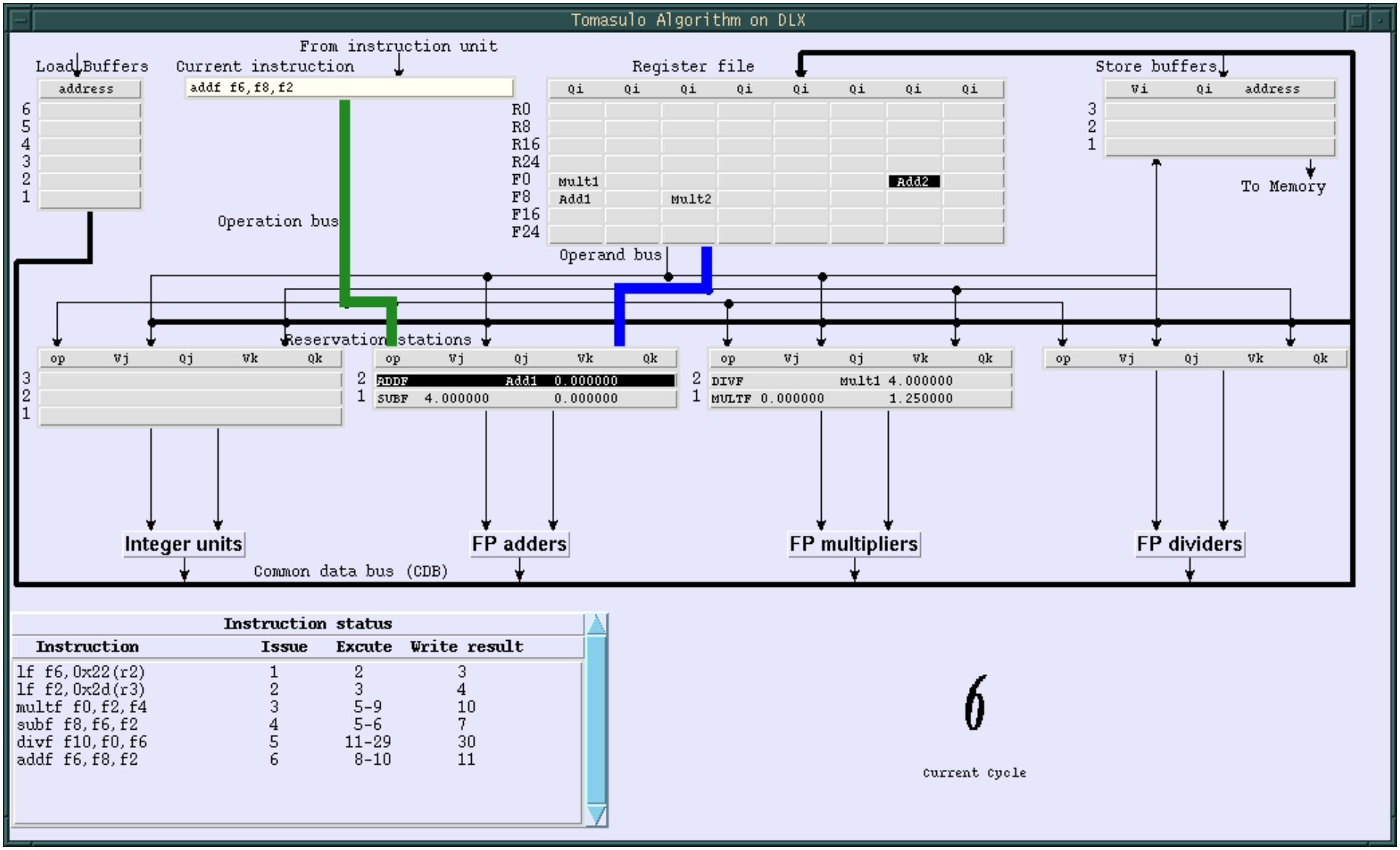

Tomasulo Algorithm on DLX
From instruction unit
Load Buffers
Current instruction
address
lf f6,0x22(r2)
6
5
4
3
2
1
(0x00000040)
Register file
Qi
R0
R8
R16
R24
F0
F8
F16
F24
Load1
Store buffers
Vi
Qi
address
To Memory
Operation bus
Operand bus
Reservation stations
op
Vj
Qj
Vk
Qk
Integer units
FP adders
FP multipliers
FP dividers
Common data bus (CDB)
Instruction status
Instruction
Issue
Excute
Write result
lf f6,0x22(r2)
1
2
3
1
Issue Cycle of Current Instruction


Tomasulo Algorithm on DLX
From instruction unit
Load Buffers
Current instruction
lf f2,0x2d(r3)
Register file
Store buffers
address
Qi
Vi
address
6
5
4
3
2
1
(0x00000044)
(0x00000040)
R0
R8
R16
R24
F0
F8
F16
F24
Load2
Load1
To Memory
Operation bus
Operand bus
Reservation stations
op
Vj
Qj
Vk
Qk
Integer units
FP adders
FP multipliers
FP dividers
Common data bus (CDB)
Instruction status
Instruction
Issue
Excute
Write result
lf f6,0x22(r2) 1 2 3
lf f2,0x2d(r3) 2 3 4
2
Current Cycle


Tomasulo Algorithm on DLX
From instruction unit
Load Buffers
Current instruction
multf f0,f2,f4
Register file
Store buffers
address
Qi
Vi
6
5
4
3
2 (0x00000044)
1 (0x00000040)
R0
R8
R16
R24
F0 Mult1 Load2 Load1
F8
F16
F24
To Memory
Operation bus
Operand bus
Reservation stations
op Vj Qj Vk Qk
MULTF Load2 1.250000
Integer units
FP adders
FP multipliers
FP dividers
Common data bus (CDB)
Instruction status
Instruction Issue Excute Write result
lf f6,0x22(r2) 1 2 3
lf f2,0x2d(r3) 2 3 4
multf f0,f2,f4 3 5-9 10
3
Current Cycle


Tomasulo Algorithm on DLX
From instruction unit
Load Buffers
Current instruction
address
subf f8,f6,f2
6
5
4
3
2 (0x00000044)
1
Operation bus
Register file
Qi Qi Qi Qi Qi Qi Qi Qi
R0
R8
R16
R24
F0 Mult1 Load2
F8 Add1
F16
F24
Operand bus
Store buffers
Vi Qi address
3
2
1
To Memory
Reservation stations
op Vj Qj Vk Qk
3
2
1
op Vj Qj Vk Qk
2
1 SUBF 4.000000 Load2
op Vj Qj Vk Qk
2
1 MULTF Load2 1.250000
op Vj Qj Vk Qk
Integer units
FP adders
FP multipliers
FP dividers
Common data bus (CDB)
Instruction status
Instruction Issue Excute Write result
lf f6,0x22(r2) 1 2 3
lf f2,0x2d(r3) 2 3 4
multf f0,f2,f4 3 5-9 10
subf f8,f6,f2 4 5-6 7
4
Current Cycle


Tomasulo Algorithm on DLX
From instruction unit
Load Buffers
Current instruction
divf f10,f0,f6
Register file
Store buffers
address
Qi
Vi
address
6
5
4
3
2
1
R0
R8
R16
R24
F0
F8
F16
F24
Mult1
Add1
Mult2
To Memory
Operation bus
Operand bus
Reservation stations
op
Vj
Qj
Vk
Qk
SUBF 4.000000 0.000000
DIVF Mult1 4.000000
MULTF 0.000000 1.250000
Integer units
FP adders
FP multipliers
FP dividers
Common data bus (CDB)
Instruction status
Instruction
Issue
Excute
Write result
lf f6,0x22(r2) 1 2 3
lf f2,0x2d(r3) 2 3 4
multf f0,f2,f4 3 5-9 10
subf f8,f6,f2 4 5-6 7
divf f10,f0,f6 5 11-29 30
5
Current Cycle

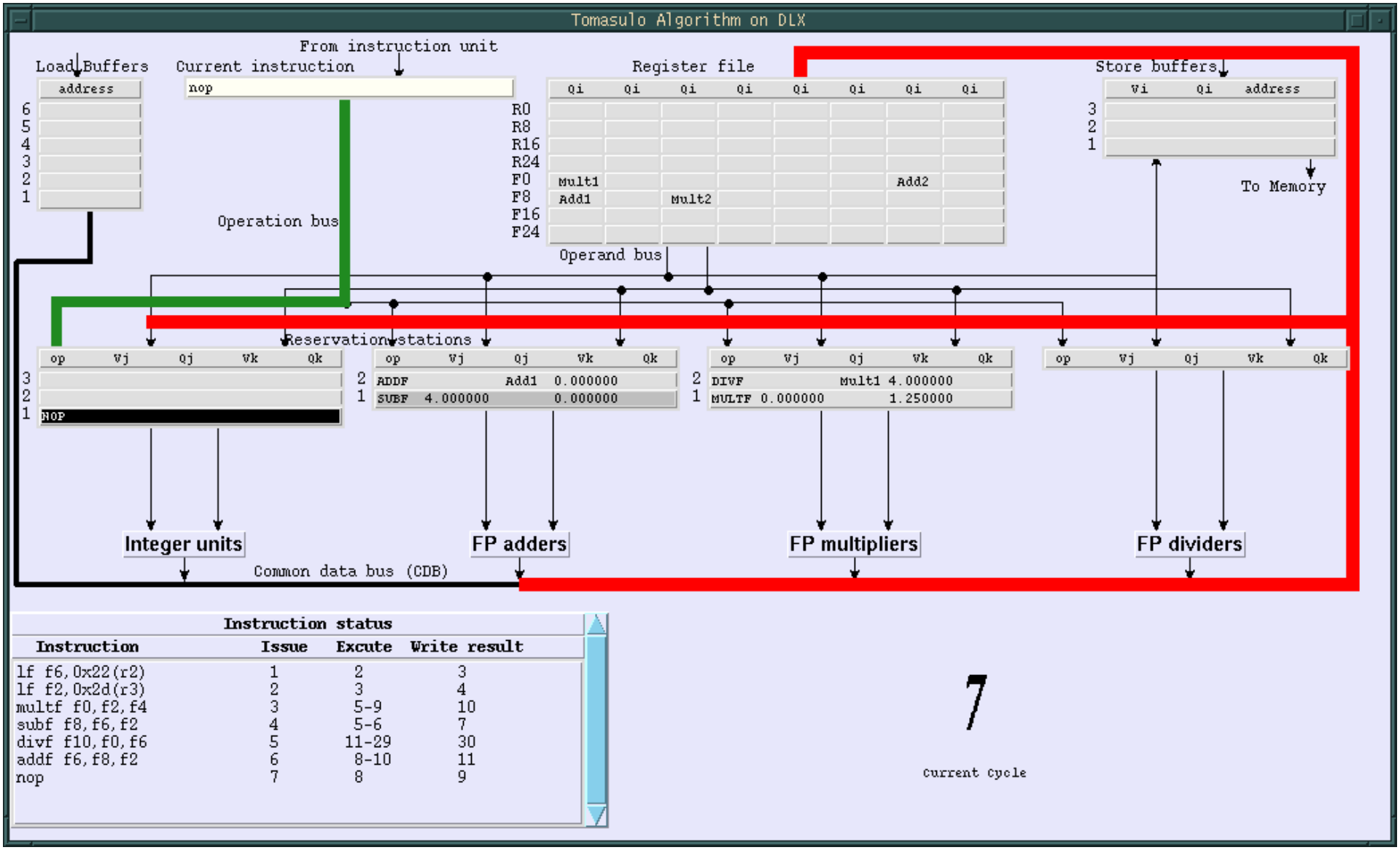


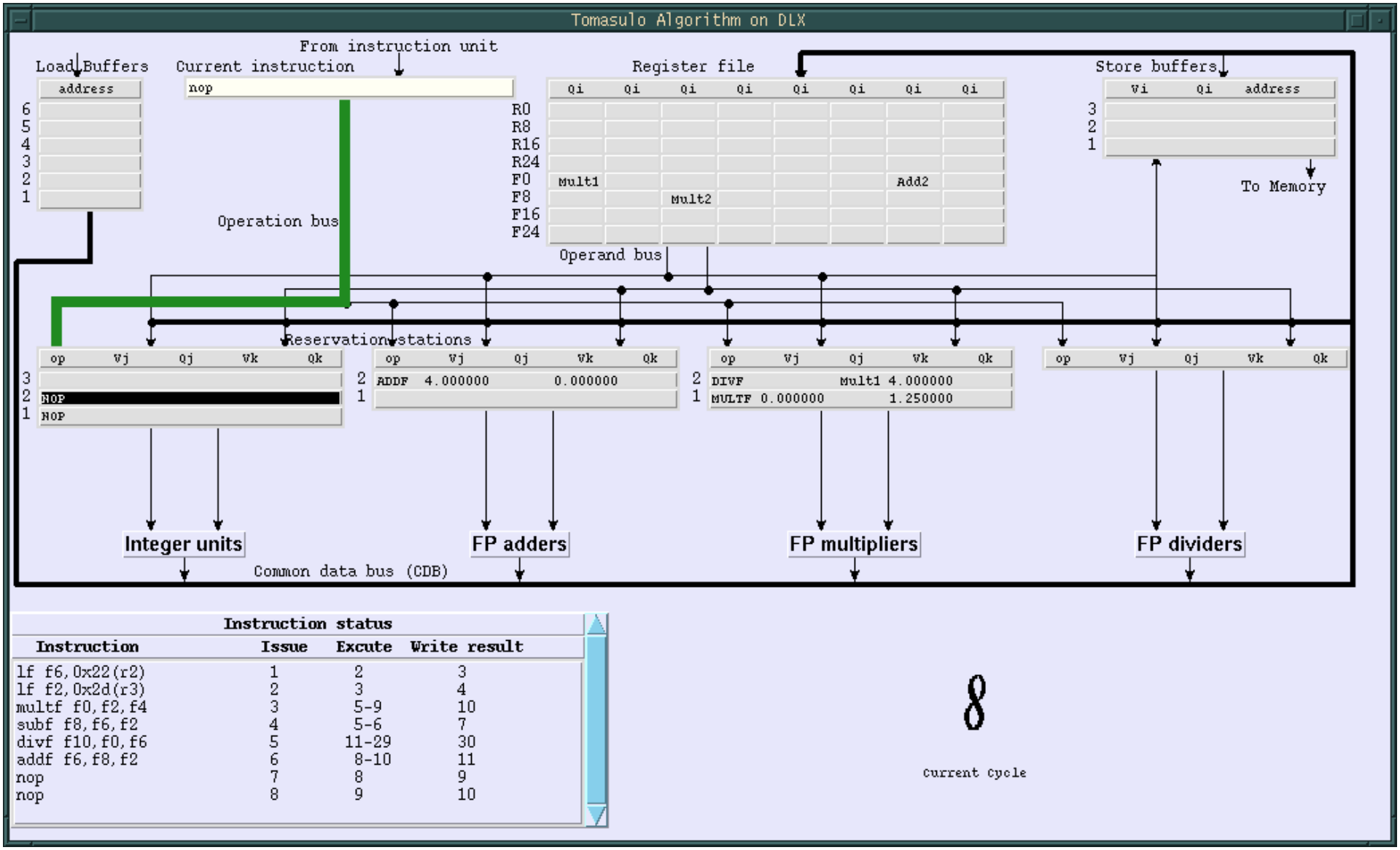
Instruction status

Instruction	Issue	Excute	Write result
lf f6,0x22(r2)	1	2	3
lf f2,0x2d(r3)	2	3	4
multf f0,f2,f4	3	5-9	10
subf f8,f6,f2	4	5-6	7
divf f10,f0,f6	5	11-29	30
addf f6,f8,f2	6	8-10	11

6

Current Cycle


Tomasulo Algorithm on DLX
From instruction unit
Load Buffers
Current instruction
nop
address
Register file
Qi
Store buffers
Vi
Qi
address
To Memory
Operation bus
Operand bus
R0
R8
R16
R24
F0
F8
F16
F24
Mult1
Add2
Add1
Mult2
Reservation stations
op
Vj
Qj
Vk
Qk
ADDF
Add1
0.000000
SUBF
4.000000
NOP
DIVF
Mult1
MULTF
Integer units
FP adders
FP multipliers
FP dividers
Common data bus (CDB)
Instruction status
Instruction
Issue
Excute
Write result
lf f6,0x22(r2) 1 2 3
lf f2,0x2d(r3) 2 3 4
multf f0,f2,f4 3 5-9 10
subf f8,f6,f2 4 5-6 7
divf f10,f0,f6 5 11-29 30
addf f6,f8,f2 6 8-10 11
nop 7 8 9
7
Current Cycle

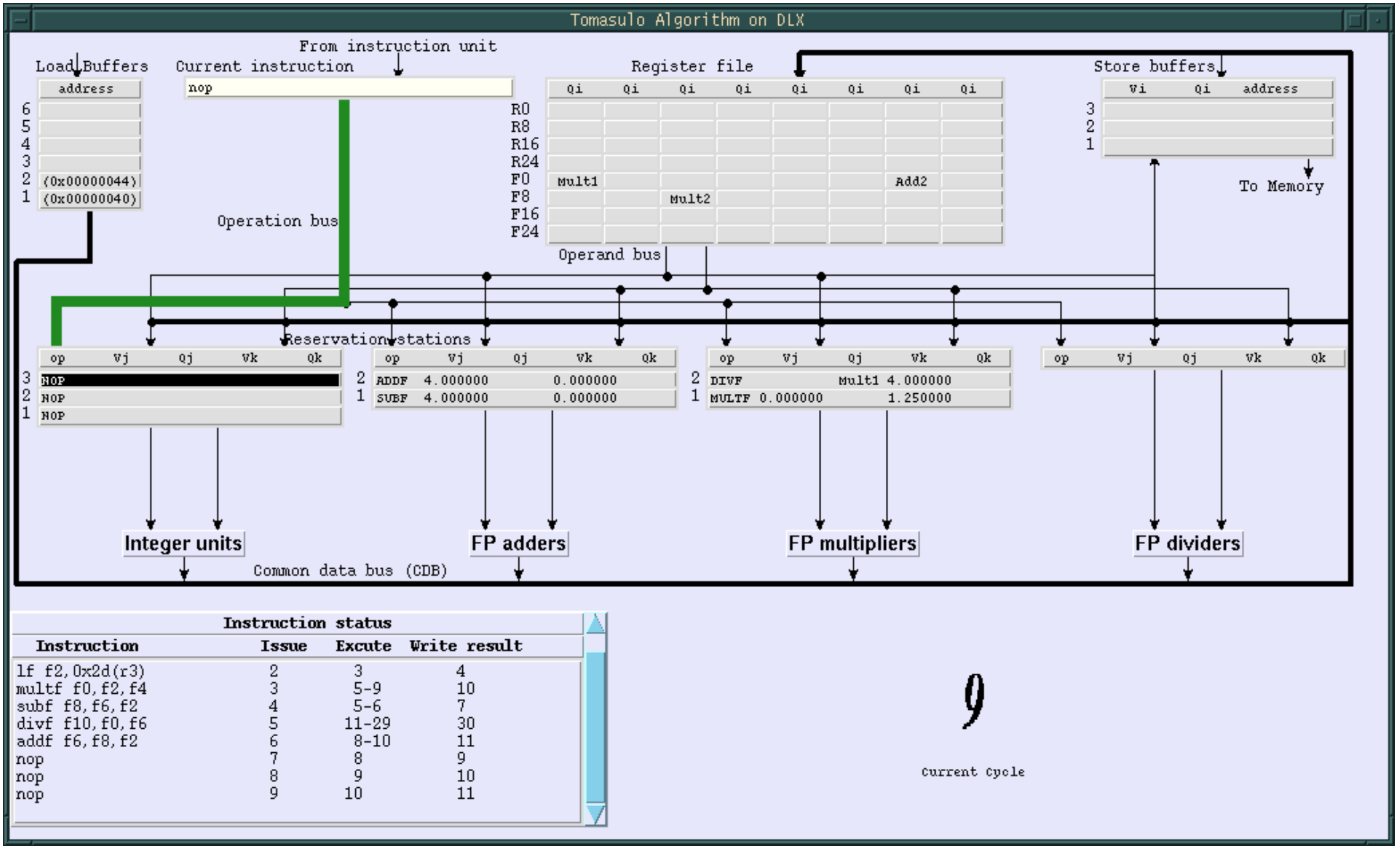


Instruction status

Instruction	Issue	Excute	Write result
lf f6,0x22(r2)	1	2	3
lf f2,0x2d(r3)	2	3	4
multf f0,f2,f4	3	5-9	10
subf f8,f6,f2	4	5-6	7
divf f10,f0,f6	5	11-29	30
addf f6,f8,f2	6	8-10	11
nop	7	8	9
nop	8	9	10

8

Current Cycle

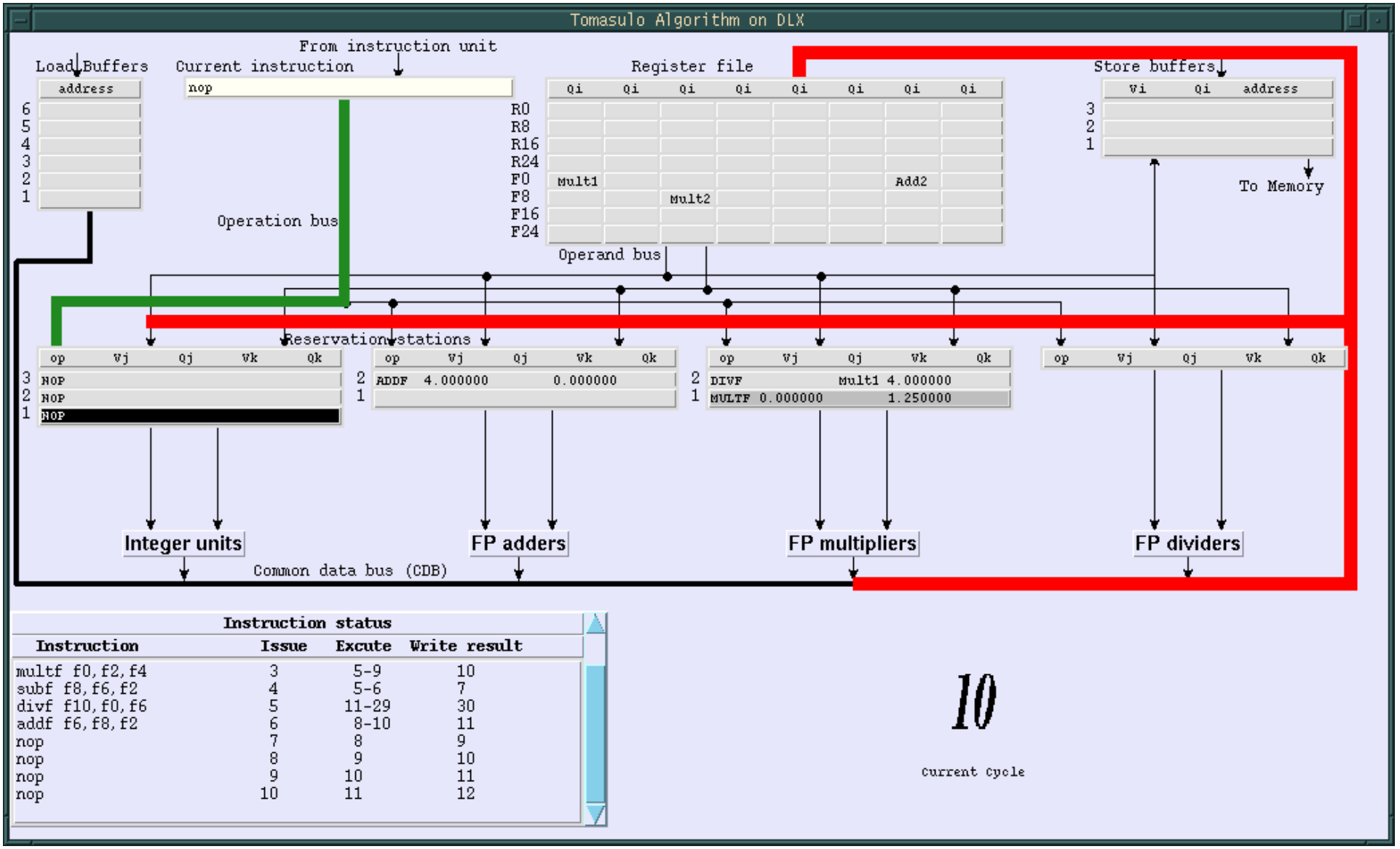


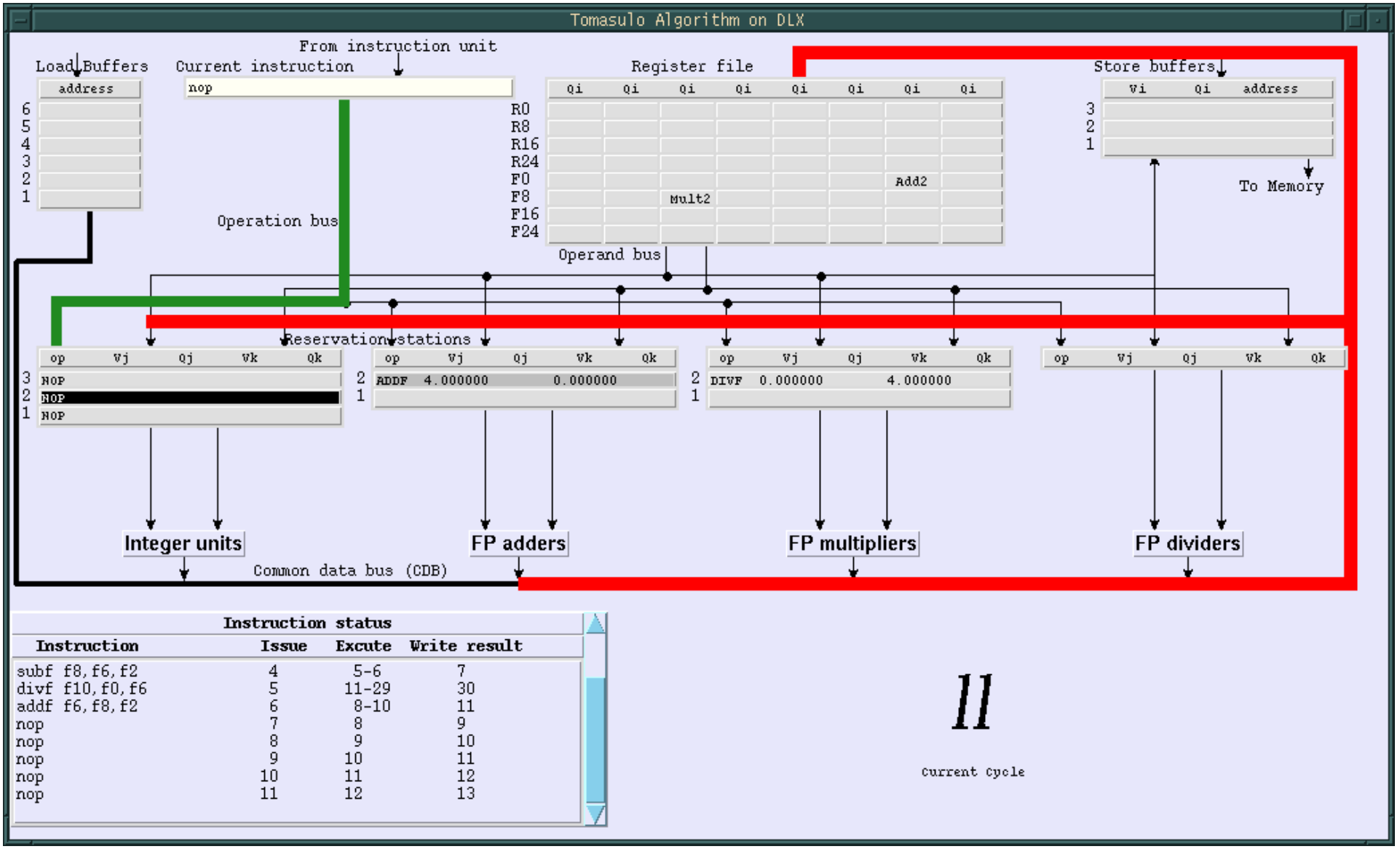
Instruction status

Instruction	Issue	Excute	Write result
lf f2,0x2d(r3)	2	3	4
multf f0,f2,f4	3	5-9	10
subf f8,f6,f2	4	5-6	7
divf f10,f0,f6	5	11-29	30
addf f6,f8,f2	6	8-10	11
nop	7	8	9
nop	8	9	10
nop	9	10	11

9

Current Cycle


Tomasulo Algorithm on DLX
From instruction unit
Load Buffers
Current instruction
nop
address
Register file
Qi
Store buffers
Vi
Qi
address
To Memory
Operation bus
Operand bus
Mult1
Mult2
Add2
Reservation stations
op
Vj
Qj
Vk
Qk
NOP
ADDF 4.000000 0.000000
DIVF Mult1 4.000000
MULTF 0.000000 1.250000
Integer units
FP adders
FP multipliers
FP dividers
Common data bus (CDB)
Instruction status
Instruction
Issue
Excute
Write result
multf f0,f2,f4 3 5-9 10
subf f8,f6,f2 4 5-6 7
divf f10,f0,f6 5 11-29 30
addf f6,f8,f2 6 8-10 11
nop 7 8 9
nop 8 9 10
nop 9 10 11
nop 10 11 12
10
Current Cycle

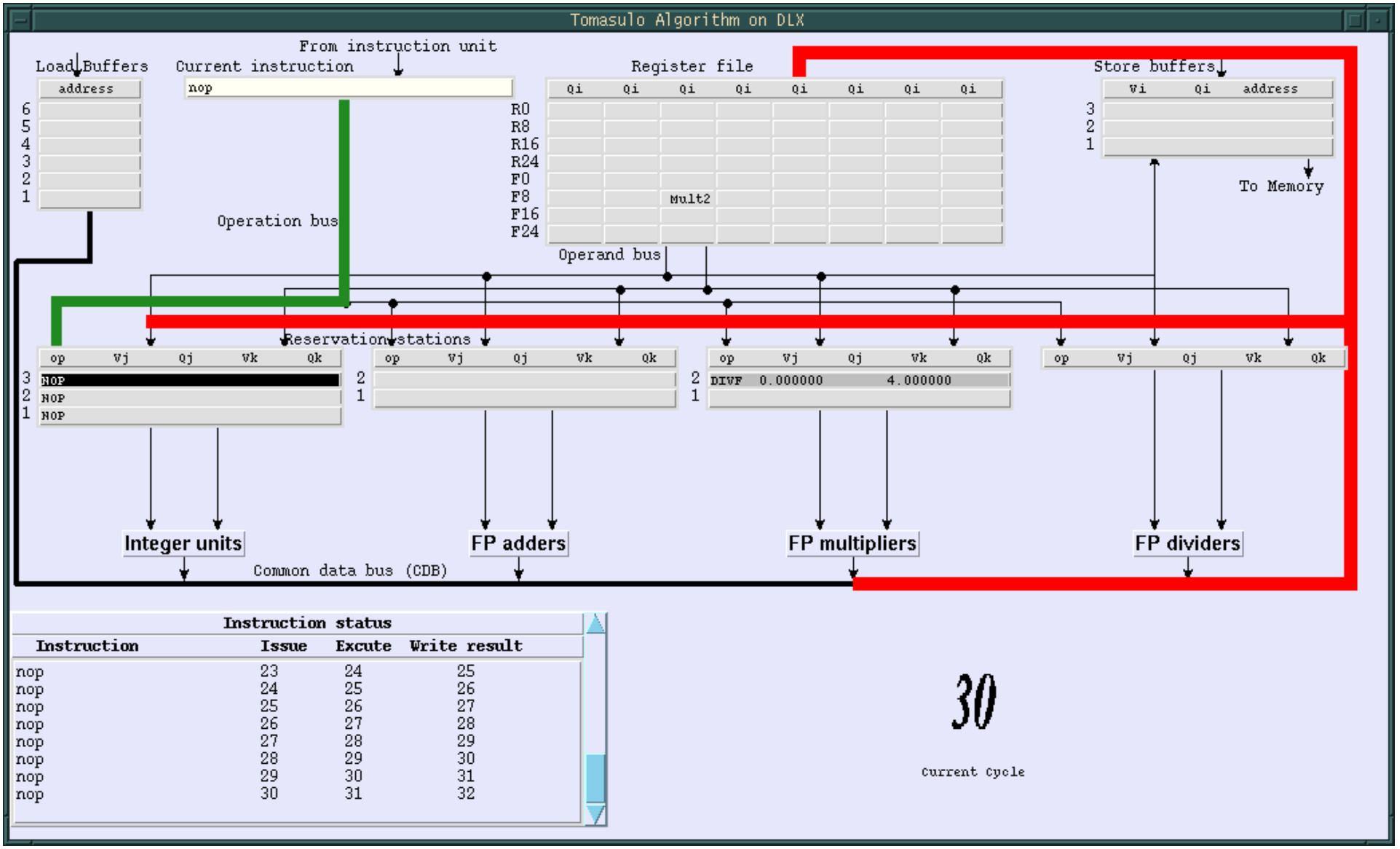


Instruction status

Instruction	Issue	Excute	Write result
subf f8, f6, f2	4	5-6	7
divf f10, f0, f6	5	11-29	30
addf f6, f8, f2	6	8-10	11
nop	7	8	9
nop	8	9	10
nop	9	10	11
nop	10	11	12
nop	11	12	13

11

Current Cycle


Tomasulo Algorithm on DLX
From instruction unit
Load Buffers
Current instruction
nop
address
Register file
Qi
R0
R8
R16
R24
F0
F8
F16
F24
Mult2
Store buffers
Vi
Qi
address
To Memory
Operation bus
Operand bus
Reservation stations
op
Vj
Qj
Vk
Qk
NOP
DIVF 0.000000 4.000000
Integer units
FP adders
FP multipliers
FP dividers
Common data bus (CDB)
Instruction status
Instruction
Issue
Excute
Write result
nop 23 24 25
nop 24 25 26
nop 25 26 27
nop 26 27 28
nop 27 28 29
nop 28 29 30
nop 29 30 31
nop 30 31 32
30
Current Cycle