True or False:

(1) (1) The relative performance of two processors with the same instruction set architecture (ISA) cannot be judged by clock rate or by the performance of a single benchmark suite.

(2) (1) Benchmarks remain valid indefinitely.

(3) (1) Peak performance does not track observed performance.

(4) (1) The best design for a computer is the one that optimizes the primary objective without considering implementation.

(5) (1) Synthetic benchmarks predict performance for real programs.

(6) (1) MIPS is an inaccurate measure for comparing performance among computers.

(7) (1) Wire delays, not transistors, are likely to be the most significant limit on clock frequency in the future.

Short Answers:

(8) (3) Most silicon dies are fairly small. Why are they not bigger? Why aren't more of them 3 inches by 3 inches, for example?

(9) (2) What was the world's first fully operational electronic general-purpose computer?

(10) (2) What does SPEC stand for?

(11) (6) List the 5 classes of benchmarks, give an example for each class, and tell me what the perfect benchmark would be.

(12) (6) There are 3 kinds of Hazards. List and give brief descriptions of all three.

(13) (6) There are 3 kinds of dependencies. List and give brief descriptions of all three.

(14) (10) Compare and contrast Tomasulo's algorithm with Scoreboarding. (Convince me you understand both - in other words, explain what they are, how they work, why they work, how they differ, how they are the same, etc.)

(15) (10) Compare and contrast Superscalar with VLIW. Describe each, and list the advantages and disadvantages of each approach.

(16) (3) What makes pipelining hard to implement? (Ignoring instruction set issues)

(17) (5) Why is branch prediction important? What performance enhancing techniques have made it so? Give 1 static and 2 dynamic branch prediction approaches (in order of increasing effectiveness).

(10) What is speculation? Is it important for high performance processors? Why? Discuss the various ramifications of supporting speculation, focusing on impacts on performance.

(18) (15) Suppose the measured branch frequencies of processor A (listed as percentages of all instructions) are as follows:

Conditional branches: 15% (60% are taken)
Jumps and calls: 1%

We are examining a four-deep pipeline where the branch is resolved at the end of the second cycle for unconditional branches and at the end of the third cycle for conditional branches. Assuming that only the first pipe stage can always be done independent of whether the branch is taken, and ignoring other pipeline stalls, how much faster would the machine be without any branch hazards?

(19) (15) Assume that a processor with a single port to memory has a clock rate that is 1.05 times higher than the clock rate of the processor with dual ported memory. Data references constitute 40% of an instruction mix, and the ideal CPI of a pipelined processor without any structural hazards is 1. Disregarding any other performance losses, is the pipeline with or without the structural hazard faster, and by how much?