1. (1pts) What is the Hamming distance between these two bit patterns: 1101 and 0111?

2. (3pts) How far apart must valid code words be to allow Single Error Detection (SED)?
   Triple Error Correction (TEC)?
   Sextuple (6) Error Correction Seven-tuple (7) Error Detection (SECSED)?

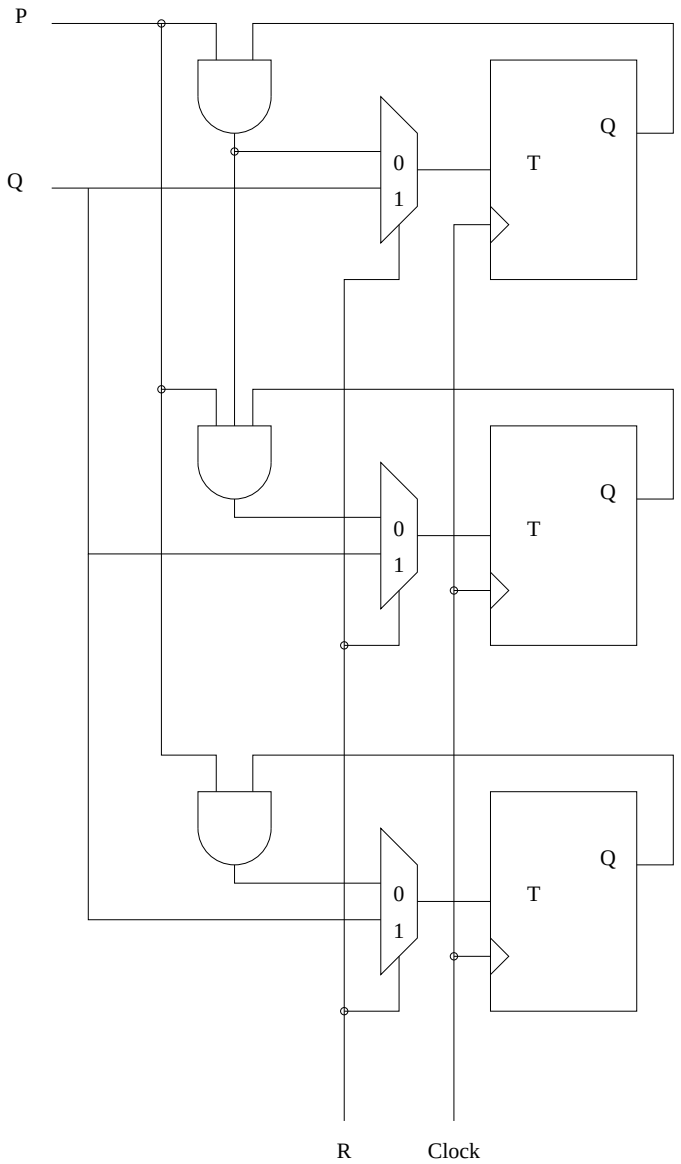
3. (3pts) Write the equation for the carry out of the 5th adder cell in an ALU using carry-lookahead, in terms of P's and G's.

4. (4pts) What is the difference between the Mealy and Moore models of sequential design?

5. (4pts) What is the difference between a Flip-Flop and a latch?

6. (10 pts) What is the maximum clock frequency possible for the following circuit? (In other words, what is the maximum clock frequency that will still guarantee correct behavior?) Use the following delay values, and assume all input signals become valid at time 0:

AND: 6 ns MUX: 8 ns Tprop: 9 ns Tsetup: 4ns Thold: 2ns



7. (10 pts) Assume you have 8-bit data words, and your memory system supports Single Error Correction. For each of the following patterns recieved from memory identify and correct any errors that may have occurred during transmission or storage. Assume the same organization of carry and data bits as we used in class. The first one is done for you.

Given: **0 0 1 0 1 1 0 1 0 1 1 1** The Data Word is: **00101011**

Given: **0 0 0 0 1 0 0 1 1 0 0 0** The Data Word is:

8. (5 pts) You have derived the following karnaugh maps for the inputs to a JK flip-flop. Unfortunately, the parts department just called and your company is completely out of JK flip-flops. All they have left in stock is Toggle flip-flops, which you will have to use instead. Show the resulting karnaugh map for the modified version of the circuit (the one that uses the Toggle instead of the JK flip-flop.)

J'

Y2 \ Y3			X	
	1		**d**	**1**
	d	**d**	**d**	**d**
	d	**d**	**d**	**d**
	1		**1**	

Y1

K'

Y2 \ Y3			X	
	d	**d**	**d**	**d**
	1			
			1	**1**
	d	**d**	**d**	**d**

Y1

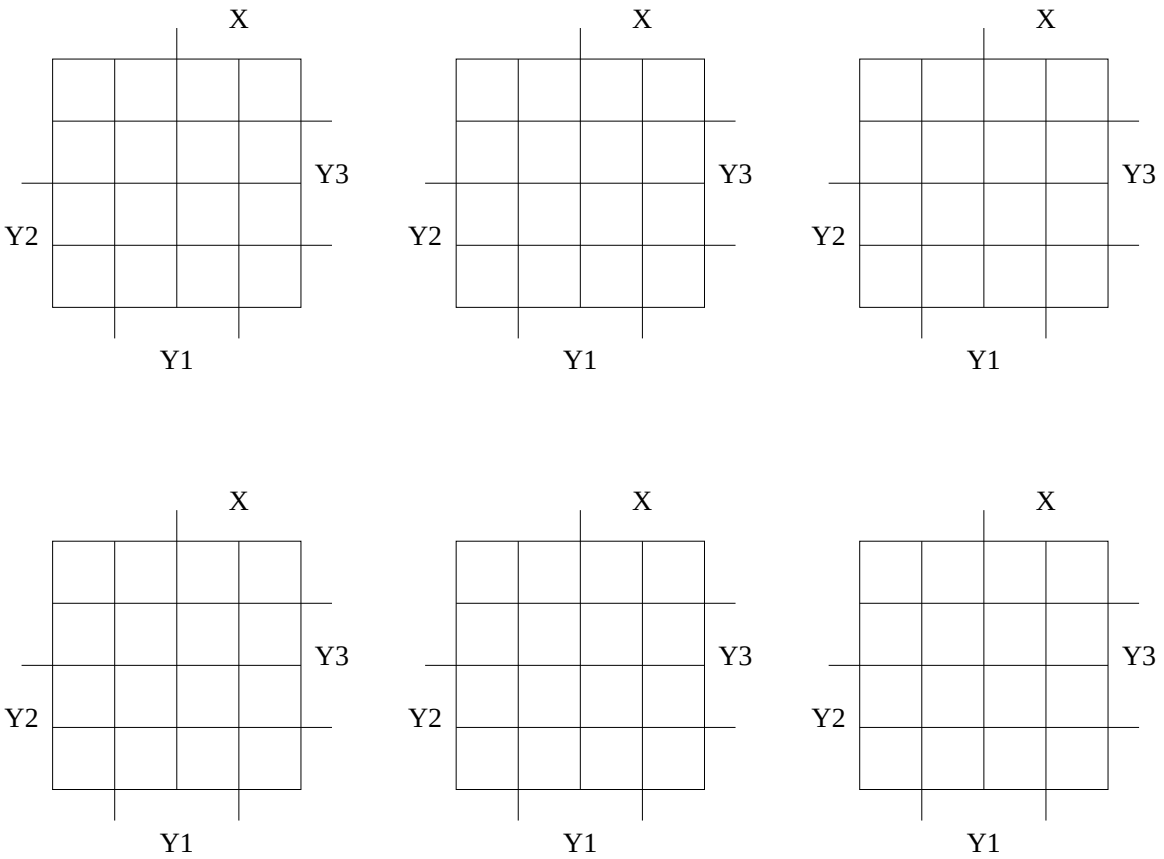
T'

Y2 \ Y3			X	

Y1

9. (20pts) Given the following table, draw the Karnaugh maps for Y1’, Y2’, and Y3’ and Z in terms of X, Y1, Y2 and Y3, and then write **minimum** boolean equations for each.

Present State (Y1 Y2 Y3)	Next State X=0 (Y1’ Y2’ Y3’)	Next State X=1 (Y1’ Y2’ Y3’)	Output (Z) X=0	Output (Z) X=1
0 0 0	1 1 0	1 1 1	1	1
0 1 0	1 0 1	1 1 1	0	0
0 1 1	1 1 1	1 1 1	1	1
1 0 0	0 0 0	1 1 0	1	0
1 0 1	0 1 1	1 1 1	1	0
1 1 0	0 0 0	0 1 0	0	0
1 1 1	0 1 1	0 1 1	1	0



10. (20 pts) Given the following Karnaugh maps, implement the sequential machine using an RS FF for Y1, a JK FF for Y2, and a Toggle FF for Y3. You do not need to draw the gates, but you do need to write down minimized input equations for each of the inputs of each of the Flip Flops in the circuit.

Y1'

Y2 \ Y3	X			
	1	1	1	1
	1			d
	1	d		1
		1	1	

Y1

Y2'

Y2 \ Y3	X			
	d		1	1
		d	1	1
			d	1
		1	1	

Y1

Y3'

Y2 \ Y3	X			
		1	1	
	1			1
	1			1
		1	1	

Y1

Y2 \ Y3	X			

Y1

Y2 \ Y3	X			

Y1

Y2 \ Y3	X			

Y1

Y2 \ Y3	X			

Y1

Y2 \ Y3	X			

Y1

Y2 \ Y3	X			

Y1

11. (20 pts) Freedonia wants to install a pay phone in the President's living area. This phone will take two coins, the 10 Moolah piece and the 20 Moolah piece. A phone call costs 50 Moolah. Since this phone will be in the President's palace, it must give change. Let X1=20 Moolah coin and X2= 10 Moolah coin, and assume both coins cannot be inserted simultaneously.

Draw the State Transistion Diagram (the circles and the arcs) for this finite state machine. Let S0=no money input (the Start state). Once you have a state transition diagram, minimize the number of states necessary and then assign bit patterns to each state and write down the corresponding state transition table. Assume you are using a Mealy model. Label the transitions on the diagram using the format we used in class (inputs over outputs).