1. (9 pts) **We're going to play Final (exam) Jeopardy!** Associate the following answers with the appropriate question. (You are given the "answers": Pick the "question" that goes best with each "answer".) The first two have been done for you.

"Answers:"

1 **(t)**. A lame attempt at humor.

2 **(u)** Anywhere but here.

3. That portion of the system bus used for the transfer of an Address.
4. A technique in which the occurance of one event on a bus follows and depends only on the occurance of a previous event.
5. To maximize the use of the expensive part of the system.
6. To make Memory appear to cost as much as the cheapest element and perform as well as the fastest element.
7. Technique used in CD-ROM Drives.
8. A technique in which an I/O device is periodically checked to see if it needs service.
9. A binary digit appended to a group of binary digits to make the sum of all the digits either always odd or always even.
10. Acts as a buffer for recently used page table contents.
11. Acts as a buffer for recently used memory contents.

"Questions:"

a) What is synchronous timing?
b) What is asynchronous timing?
c) What is a Cache?
d) What is a Address Translation Lookaside Buffer?
e) What is the Address Bus?
f) What is the Data Bus?
g) What is a Parity error?
h) What is a Register?
i) What is DMA?
j) What is an interrupt?
k) What is a Page?
l) What is a Floating Point number?
m) What is a Page Fault?
n) What is a Parity bit?
o) What is a Sign bit?
p) What is the goal of the Memory Heirarchy?
q) What is polling?
r) What is the goal of multiprogramming?
s) What is Constant Linear Velocity?
u) What is this question?
v) Where would I rather be right now than where I am?

2. (3) What is the difference between memory access time and memory cycle time?

3. (3) What is the difference between volatile and non-volatile memory?

4. (3) What is the goal of the Memory Heirarchy?

5. (4) What is a TLB, and what is it used for?

6. (4) Explain the principle of Locality and why it is important.

7. (4) Which one should you buy, a 120MHZ Pentium or a 200MHZ Alpha? Why? How do you decide which is faster, and which one is best for you?

8. (6) Given a 20-bit address and a 16K-byte physical memory,

How big is the virtual address space?

How big is the physical address space?

Assuming 512-byte pages, how many page frames are there? How many pages?

Assuming 2K-byte pages, how many page frames are there? How many pages?

9. (3 pts) For the following 8-bit patterns, add a 9th bit to create:

Even Parity: 10011110_

Odd Parity: 00100111_

What is the Hamming distance between these two codewords?

10. (8 pts) Here is a 12-bit Error Correction code format (same one used in class):

$$d_8\ d_7\ d_6\ d_5\ C_4\ d_4\ d_3\ d_2\ C_3\ d_1\ C_2\ C_1$$

a. Given the *data* bit pattern

1 0 0 1 0 1 1 0

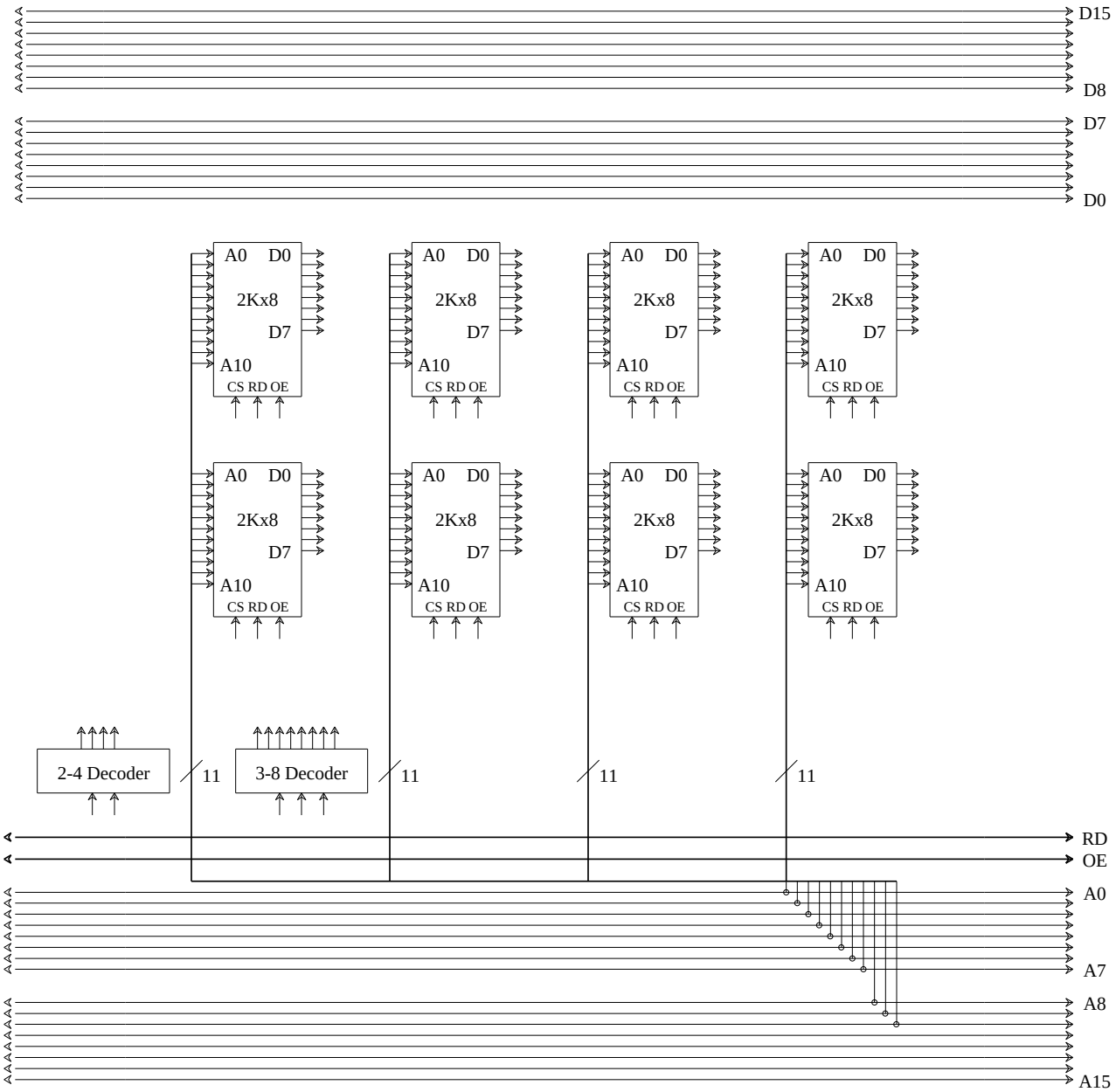
in a machine using the above ECC code, what bit pattern gets sent to memory?

b. In this same machine, the following bit pattern is retrieved from memory:

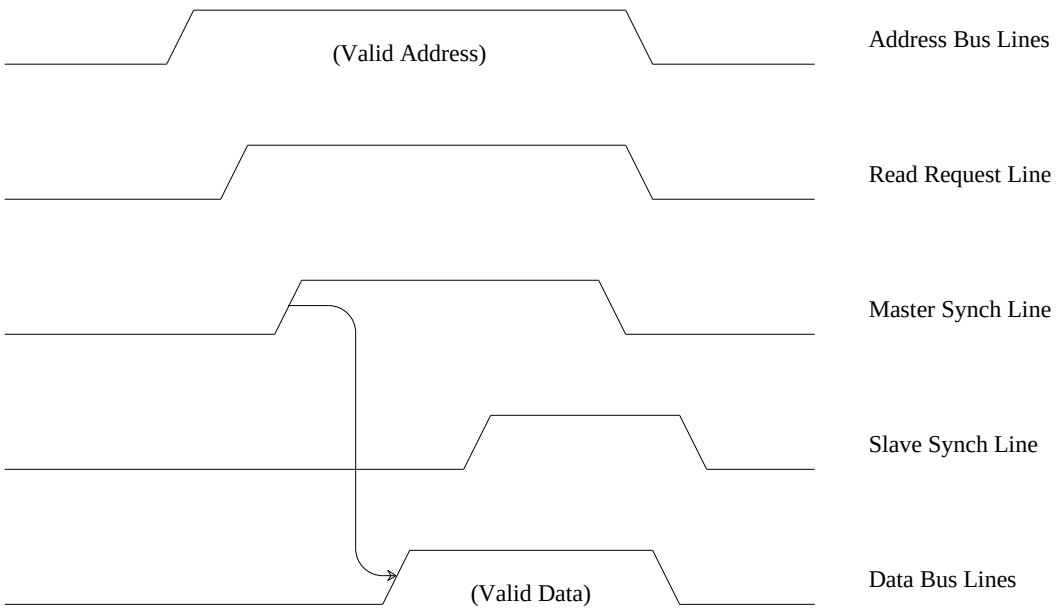
0 0 0 0 0 0 0 0 0 0 1 0

Assuming the above Error Correction code format, identify and correct any errors that may have occurred during transmission or storage.

11. (10 pts) Add the connections to the following diagram necessary to create an 8Kx16 memory. Note - Not all of the hardware shown is required to perform this task.



12. (10 pts) Add arrows to the following diagram to indicate which signal transitions cause other transitions to occur. The first one has been done for you.



Now explain in words (briefly) what the arrows you have added are doing. (What is the sequence of events in words?)

13. (12 pts) Given a 32-byte Direct Mapped Cache with a line size of 2 words, a word size of 16 bits, a 128-byte memory containing the values shown, and the following address reference sequence for a byte-addressable machine:

0x0E,0x1A,0x0C,0x26,0x06

Fill in the Cache's Tag and Data values after each memory reference has been processed. Assume all the entries in the tag array are initially invalid.

Memory Contents at Address **XY**																
Most Significant Digit(**X**)	Least Significant Digit (**Y**)															
	0	1	2	3	4	5	6	7	8	9	a	b	c	d	e	f
0	23	20	6d	61	74	74	27	73	20	67	76	69	65	77	20	73
1	68	65	6c	6c	20	73	63	72	69	70	74	0a	73	65	74	20
2	67	66	69	6c	65	20	3d	20	24	31	0a	09	65	63	68	6f
3	20	2d	6e	20	22	67	67	72	61	70	68	20	24	67	66	69
4	6c	65	2e	2e	2e	22	20	0a	09	65	63	68	6f	20	22	2e
5	73	70	20	32	22	20	3e	21	20	2f	74	6d	70	2f	74	65
6	6d	70	24	24	2e	6e	72	0a	09	65	63	68	6f	20	22	2e
7	70	6f	20	2b	30	2e	35	69	22	20	3e	3e	20	2f	74	6d

Tag Array	Contents of Tag Array after processing address (Time ->)				
Address	0E	1A	0C	26	06
0					
1					
2					
3					
4					
5					
6					
7					

Data Array	Contents of Data Array after processing address (Time ->)				
Address	0E	1A	0C	26	06
0					
1					
2					
3					
4					
5					
6					
7					

14. (14 pts) Given a 32-byte 2-way Set Associative Cache with a line size of 2 words, a word size of 16 bits, a 128-byte memory containing the values shown, and the following address reference sequence for a byte-addressable machine:

0x0E,0x36,0x1A,0x0C,0x26,0x06

Use an LRU replacement scheme.

Memory Contents at Address **XY**																
Most Significant Digit(**X**)	Least Significant Digit (**Y**)															
	0	1	2	3	4	5	6	7	8	9	a	b	c	d	e	f
0	23	20	6d	61	74	74	27	73	20	67	76	69	65	77	20	73
1	68	65	6c	6c	20	73	63	72	69	70	74	0a	73	65	74	20
2	67	66	69	6c	65	20	3d	20	24	31	0a	09	65	63	68	6f
3	20	2d	6e	20	22	67	67	72	61	70	68	20	24	67	66	69
4	6c	65	2e	2e	2e	22	20	0a	09	65	63	68	6f	20	22	2e
5	73	70	20	32	22	20	3e	21	20	2f	74	6d	70	2f	74	65
6	6d	70	24	24	2e	6e	72	0a	09	65	63	68	6f	20	22	2e
7	70	6f	20	2b	30	2e	35	69	22	20	3e	3e	20	2f	74	6d

Tag Array		Contents of Tag Array after processing address (Time ->)					
Set	Address	0E	36	1A	0C	26	06
0	0						
	1						
1	2						
	3						
2	4						
	5						
3	6						
	7						

Data Array	Contents of Data Array after processing address (Time ->)					
Address	0E	36	1A	0C	26	06
0						
1						
2						
3						
4						
5						
6						
7						

15. (12 pts) The following tables contain information about a segmented, paged virtual memory system and certain select memory locations. Total physical memory size is 2K bytes. All numbers in this table are in Hex unless otherwise noted.

Segment Table		
Entry Number	Presence Bit	Page Table
0	1	1
1	0	0

Page Table 0			
Entry Number	Presence Bit	Disk Address	Physical Page Number
0	1	1234123	0x0
1	0	0893748	0x3
2	1	2489567	0x1
3	1	9623873	0x2

Page Table 1			
Entry Number	Presence Bit	Disk Address	Physical Page Number
0	1	1234123	0x1
1	0	0893748	0x0
2	1	2489567	0x3
3	1	9623873	0x2

Memory	
Address	Contents
0x03A4	0x7230
0x05A4	0x86a9
0x06A4	0x9723
0x07A4	0x3423
0x0AA4	0x8876
0x0FA4	0x2373
0x11A4	0x1346
0x17A4	0x6792
0x1EA4	0x5292
0x37A4	0x7974
0x3BA4	0x3205
0x67A4	0x6623

Assuming 512-byte pages, convert the virtual address **0x7A4** into a physical address. (**0x7A4** is **0 1 1 1 1 0 1 0 0 1 0 0** in binary).

What is the value in memory stored at the physical address corresponding to the virtual address **0x7A4**?

(15) Given the following table, draw the Karnaugh maps for Y1', Y2', and Y3' in terms of X, Y1, Y2 and Y3, and then write minimum boolean equations for each. Please use the format for K-maps used in class.

Present State	Next State		Output	
	X=0	X=1	X=0	X=1
000	000	001	0	0
001	010	011	1	0
010	101	101	0	1
011	111	110	1	0
101	001	010	1	0
110	011	010	0	1
111	101	111	1	1