1. (2) What is DMA?

2. (3) What is the difference between memory access time and memory cycle time?

3. (4) Caches can be either Virtually Addressed or Physically Addressed. Explain the difference, and give an advantage and a disadvantage for each.

4. (4) Describe CAV (Constant Angular Velocity), CLV (Constant Linear Velocity), how they differ, and which device uses them.

5. (4) What is a TLB, and what is it used for?

6. (4) Explain the principle of Locality and why it is important.

7. (6) Given a logical 22-bit address and a 64K-byte physical memory for a byte-addressable machine,

   How big is the virtual address space?

   How big is the physical address space?

   Assuming 512-byte pages, how many page frames are there? How many pages?

   Assuming 8K-byte pages, how many page frames are there? How many pages?

8. (3 pts) For the following 8-bit patterns, add a 9th bit to create:

   Even Parity: 11011011_

   Odd Parity: 01101101_

   What is the Hamming distance between these two codewords?

9. (8 pts) Here is a 12-bit Error Correction code format (same one used in class):

$$d_8\ d_7\ d_6\ d_5\ C_4\ d_4\ d_3\ d_2\ C_3\ d_1\ C_2\ C_1$$

   a. Given the *data* bit pattern

      0 1 0 1 1 0 1 0

   in a machine using the above ECC code, what bit pattern gets sent to memory? (No credit will be given without work being shown.)

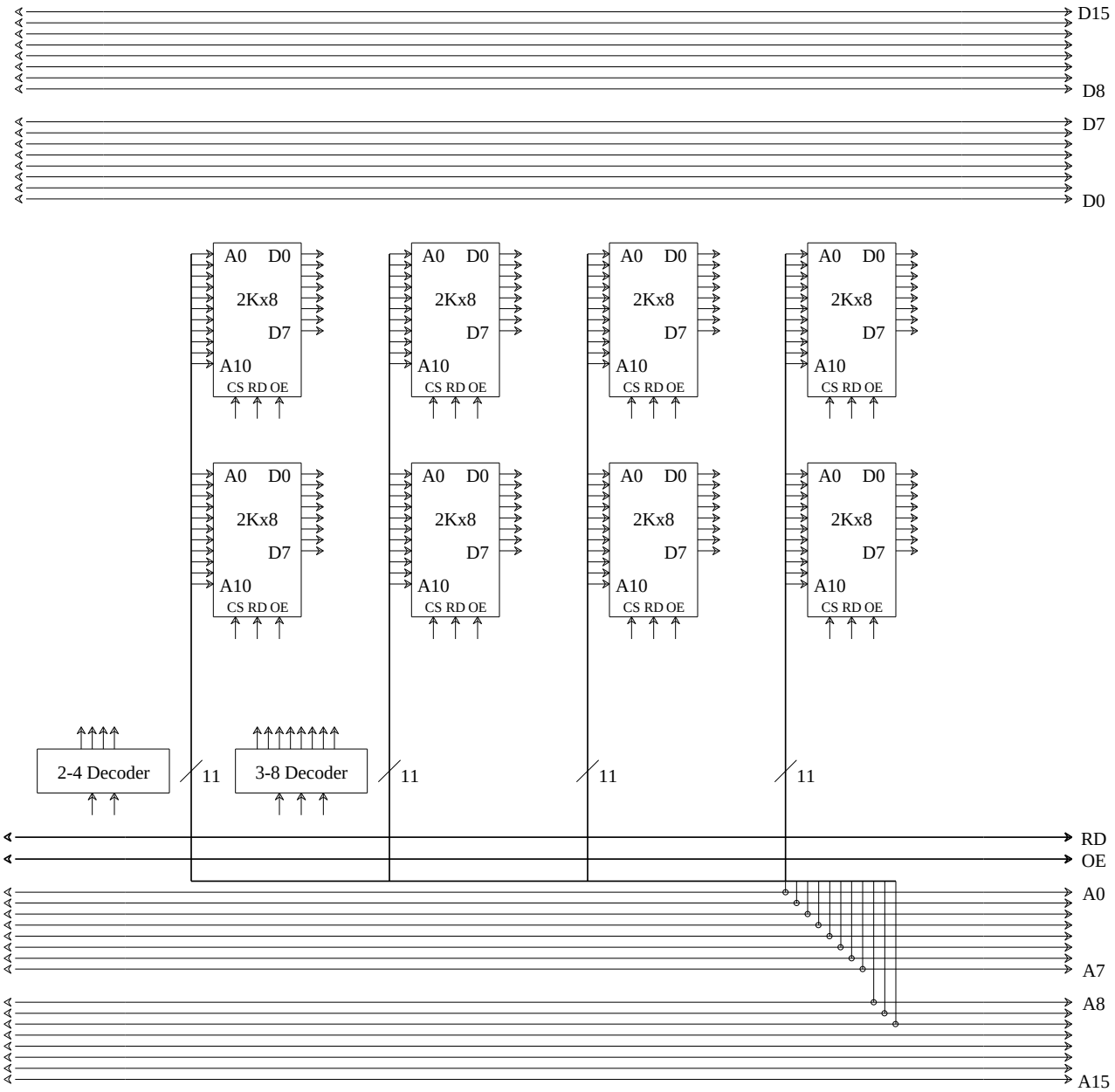
   b. In this same machine, the following bit pattern is retrieved from memory:

      0 0 1 1 0 1 1 1 0 1 1 0

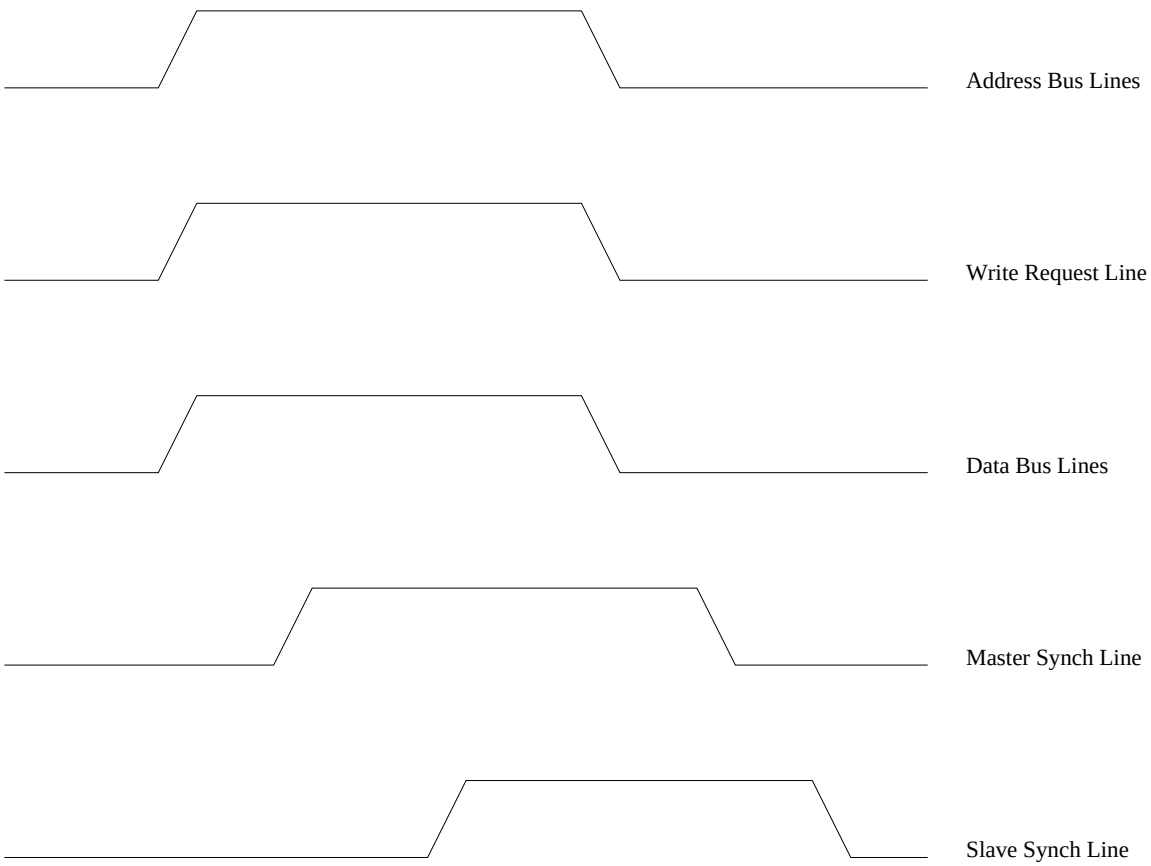
   Assuming the above Error Correction code format, identify and correct any errors that may have occurred during transmission or storage. (No credit will be given without work being shown.)

10. (8 pts) Add the connections to the following diagram necessary to create an 8Kx16 memory. Not all of the hardware shown is required to perform this task.

    CS - Chip Select
    OE - Output Enable
    RD - Read (Read/Write, technically)



11. (7 pts) Add arrows to the following diagram to indicate which signal transitions **cause** other transitions to occur.



Now explain in words (briefly) what the arrows you have added are doing. (What is the sequence of events in words?)

12. (25) Megatron Corporation makes the "Megamax Infinity", a byte-addressable computer with a 32-bit word size. In this machine the bus to main memory is 64 bits wide, and accessing Main memory takes 5 clock cycles. In order to improve performance, they are considering adding a 64-byte Direct-Mapped cache with a line size of 2 words and an access time of 1 cycle. Given the following address reference sequence (in Hex):

0xB5,0x16,0x7D,0x12,0xE1

a) Write down how you are partitioning each address (which bits are the Tag, offset, etc.)

b) In the table below, fill in the proposed Cache's Tag values after each memory reference has been processed. If it is a hit, mark the entry number to indicate this, and if it is a miss enter what the new tag should be.

Tag Array	Contents of Tag Array after processing address (Time ->)					
Entry Number	Initial Contents	0xB5 (10110101)	0x16 (00010110)	0x7D (01111101)	0x12 (00010010)	0xE1 (11100001)
0	10					
1	01					
2	11					
3	10					
4	00					
5	01					
6	10					
7	01					

What is the Average Memory access time for this sequence of references?

Now fill in the contents of the Data array after processing the given address references. (In order to save time, only a subset of the data array is given here.) The last page of the test shows the contents of memory.

Data Array	Data Array Contents after processing address	
Entry Number	0xB5	0x7D
5		
6		
7		

13. (22) Megatron decided to experiment with using a 48-byte 3-way Set Associative Cache with a line size of 1 word (instead of the Direct-mapped Cache). Remember, the Megamax Infinity is a byte-addressable machine with a 32-bit word size, a 64-bit bus to main memory, and a Main Memory access time of 5 cycles. The Cache access time is still 1 cycle. Given the same address reference sequence (in Hex) as before:

0xB5,0x16,0x7D,0x12,0xE1

a) Write down how you are partitioning each address (which bits are the Tag, offset, etc.)

b) In the table below, fill in the proposed Cache's Tag values after each memory reference has been processed. If it is a hit, mark the entry number to indicate this, and if it is a miss enter what the new tag should be. Use an LRU replacement scheme.

Tag Array			Contents of Tag Array after processing address (Time ->)					
Set Number	Entry Number	Age	Initial Contents	B5 (10110101)	16 (00010110)	7D (01111101)	12 (00010010)	E1 (11100001)
0	0		0 1 1 0					
	1	oldest	1 1 0 1					
	2	newest	0 0 1 1					
1	0	oldest	0 0 1 0					
	1		1 0 0 1					
	2	newest	1 0 1 1					
2	0	oldest	0 1 1 0					
	1	newest	0 0 1 1					
	2		1 1 0 0					
3	0		0 1 1 1					
	1	newest	0 0 0 0					
	2	oldest	0 1 0 0					

What is the Average Memory access time for this sequence of references?

14. (12 pts) The following tables contain information about a segmented, paged virtual memory system and certain select memory locations. Total physical memory size is 8K bytes, and the page size is 1K bytes. All numbers in this table are in Hex unless otherwise noted.

Segment Table

Entry Number	Presence Bit	Page Table
0	1	3
1	0	0
2	1	1
3	1	2

Memory

Address	Contents
0x00A4	0x76
0x01A4	0x73
0x05A4	0x32
0x11A4	0x46
0x13A4	0x30
0x1AA4	0x29
0x23A4	0xa9
0x29A4	0x74
0x3BA4	0x05
0x4BA4	0x23
0x4DA4	0xE3
0x67A4	0xAE
0x70A4	0x92

Page Table 0

Entry Number	Present? (1=Yes)	Disk Addr	Frame Number
0	1	1234123	0x4
1	0	0893748	0x7
2	1	2489567	0x1
3	1	9623873	0x5
4	1	AE76BD3	0x2
5	0	328759A	0x3
6	1	56D87AC	0x0
7	1	10A876D	0x6

Page Table 1

Entry Number	Present? (1=Yes)	Disk Addr	Frame Number
0	1	1234123	0x2
1	0	0893748	0x3
2	0	2489567	0x4
3	1	9623873	0x4
4	1	AE76BD3	0x6
5	0	328759A	0x7
6	1	56D87AC	0x0
7	1	10A876D	0x6

Page Table 2

Entry Number	Present? (1=Yes)	Disk Addr	Frame Number
0	1	1234123	0x1
1	0	0893748	0x3
2	1	2489567	0x5
3	1	9623873	0x7
4	1	AE76BD3	0x1
5	0	328759A	0x2
6	1	56D87AC	0x4
7	1	10A876D	0x6

Page Table 3

Entry Number	Present? (1=Yes)	Disk Addr	Frame Number
0	1	1234123	0x3
1	0	0893748	0x6
2	1	2489567	0x1
3	1	9623873	0x2
4	1	AE76BD3	0x4
5	0	328759A	0x2
6	1	56D87AC	0x5
7	1	10A876D	0x6

For each of the following convert the virtual address into a physical address (if possible) and write down the value of the memory location corresponding to the address. If it is not possible to do so, explain why.

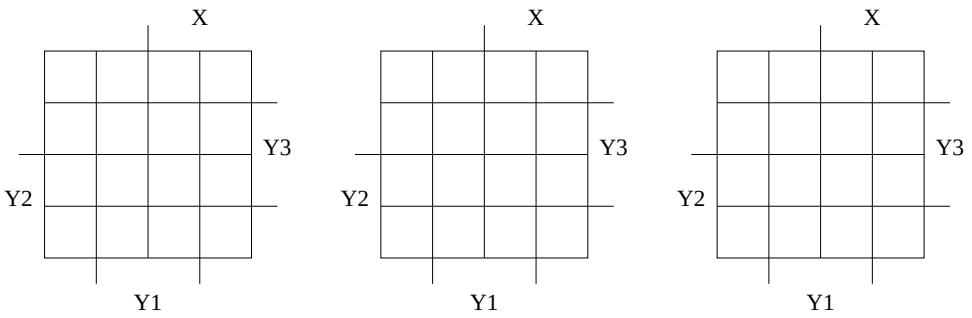
0x30A4 (**0 1 1 0 0 0 0 1 0 1 0 0 1 0 0** in binary).

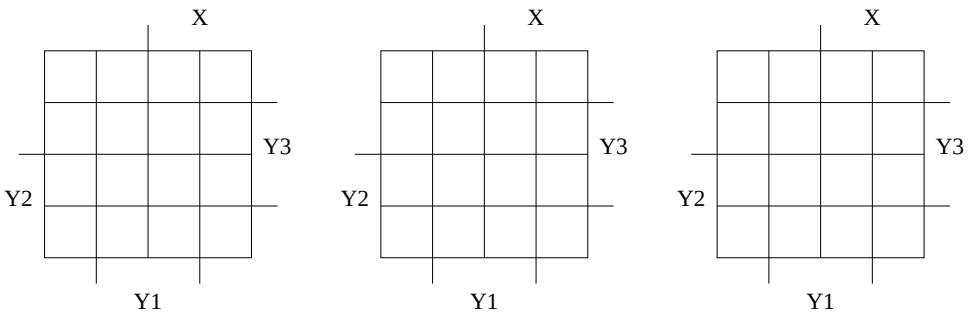
0x1EA4 (**0 0 1 1 1 1 0 1 0 1 0 0 1 0 0** in binary).

0x71A4 (**1 1 1 0 0 0 1 1 0 1 0 0 1 0 0** in binary).

15. (18) Given the following table, draw the Karnaugh maps for Y1', Y2', and Y3' and Z in terms of X, Y1, Y2 and Y3, and then write **minimum** boolean equations for each.

Present State (Y1 Y2 Y3)	Next State X=0 (Y1' Y2' Y3')	Next State X=1 (Y1' Y2' Y3')	Output X=0	Output X=1
001	011	011	1	0
010	101	101	0	1
011	111	110	1	0
100	100	110	0	0
101	001	010	1	0
110	001	010	0	1
111	101	111	1	1





16. (20 pts) Given the following Karnaugh maps, implement the sequential machine using an SR FF for Y1, a JK FF for Y2, and a T FF for Y3. You do not need to draw the gates, but you do need to write down the **minimized** input equations for each of the inputs of each of the Flip Flops in the circuit.

Y1'

Y2 \ Y3	X			
	1			1
	1	1	1	1
		1	1	

Y1

Y2'

Y2 \ Y3	X			
	1	1	1	1
		d	1	
		1	1	
	1			1

Y1

Y3'

Y2 \ Y3	X			
	1	1		
		1	1	
		1	1	
			1	1

Y1

Y2 \ Y3	X			

Y1

Y2 \ Y3	X			

Y1

Y2 \ Y3	X			

Y1

Y2 \ Y3	X			

Y1

Y2 \ Y3	X			

Y1

Memory Contents (for question 12).

Memory Contents at Hex Address **XY**																
Most Significant Digit (**X**)	Least Significant Digit (**Y**)															
	0	1	2	3	4	5	6	7	8	9	a	b	c	d	e	f
0	23	20	6d	61	74	74	27	73	20	67	76	69	65	77	20	73
1	68	65	6c	6c	20	73	63	72	69	70	74	0a	73	65	74	20
2	67	66	69	6c	65	20	3d	20	24	31	0a	09	65	63	68	6f
3	20	2d	6e	20	22	67	67	72	61	70	68	20	24	67	66	69
4	6c	65	2e	2e	2e	22	20	0a	09	65	63	68	6f	20	22	2e
5	73	70	20	32	22	20	3e	21	20	2f	74	6d	70	2f	74	65
6	6d	70	24	24	2e	6e	72	0a	09	65	63	68	6f	20	22	2e
7	70	6f	20	2b	30	2e	35	69	22	20	3e	3e	20	2f	74	6d
8	23	7b	92	08	22	41	85	32	69	73	11	35	97	54	31	48
9	88	73	48	72	98	21	42	85	62	65	90	84	31	56	55	83
a	43	64	84	36	59	3c	8a	95	3b	8f	0e	41	7a	40	2b	3c
b	4c	d4	c7	82	a0	38	f9	c6	29	a3	d0	9c	7d	41	2b	75
c	54	69	9c	3b	b0	2a	d9	3e	45	72	6e	f0	f9	3f	a0	0a
d	60	89	43	d8	c0	e7	49	76	59	21	2c	c8	a8	f2	87	43
e	76	8f	2e	a9	ff	38	ae	65	dd	cf	21	84	ce	e4	34	51
f	8a	65	30	2f	c9	3a	58	72	3e	a0	4f	38	96	47	21	80