ECS154A Midterm Review

Midterm is Comprehensive. What should you know? Everything in Appendix A of book, plus what was covered in class. If you have done your homework and the lab assignments, you should be in good shape.

Midterm will be closed book, but you can bring along 1 page of notes. As stated in class, emphasis will be on how well you know the material, and in particular how well you can solve problems. Expect to see a problem very much like the one we did at the end of last week, because it encompasses most of what we have done so far.

Review of what we have covered so far:

Boolean Logic

Basic gates and operations

AND, OR, XOR, NOT, NAND, NOR, etc.
What is a functionally complete set of gates?

Boolean Algebra

Identities
Axioms
Theorem (DeMorgans)
Truth Tables
Minterms, Maxterms
SOP, POS forms of equations
Minimizing equations

Karnaugh maps

What they are
How they are related to Truth tables
How and why they are used

Standard Combinational Circuits

Decoder
Encoder
Multiplexer
Demultiplexer
Adder (with and without Carry-lookahead)
Timing of combinational circuits (gate delays)

Designing Combinational circuits

- Using basic gates
- Using PLAs
- Using ROMs
- Using decoders

Synthesis of Combination Circuits

Adders

- Half-adders
- Full adders
- Ripple-carry adders
- Adders using carry-lookahead
- ALU’s (Arithmetic Logic Units that do more than just add) (P’s & G’s)

Codes

- Hamming distance
- BCD Code

Error Detection/Correction

- Parity
- M-detection N-correction concepts
- SECDED

Basics of Sequential Logic

- What it is
- Why it matters
- Present State, Next state
- Difference between Latch and Flip-Flop
- Synchronous vs. Asynchronous sequential circuits
- State Transition Tables
- Cross-coupled NANDs, NORs

Types of sequential circuits (Latches, FFs)

- Gated Latch
- RS Latch, FF
- JK FF
- Master-Slave FF
- Edge-triggered FF
- Toggle FF
- How to create one type using another (JK from RS)
- States

Design of Sequential circuit

- Model Specifications
- State Diagram
- Minimize States
- Create State Transition Table
- Select FF's to be used
- Design the logic

Creating Sequential Circuit using various types of FF's

- Transition Table
- Karnaugh Map representation