1. (2pts) Show how to make an SR latch using only NOR gates.

2. (3pts) Implement the following circuit using 6 or fewer 2-input NAND gates. Assume the variables and their complements are available.

   $A\overline{B}+B\overline{C}+AC$

3. (1pts) What is the Hamming distance between these two bit patterns: 1011 and 0111?

4. (3pts) How far apart must valid code words be to allow Single Error Detection (SED)?
   Double Error Correction (DEC)?
   Triple (3) Error Correction Quadruple (4) Error Detection (TECQED)?

5. (2pts) Write the equation for the carry into the 4th adder cell in an ALU using carry-lookahead, in terms of P's and G's.

6. (2pts) What is the difference between a Flip-flop and a Latch?

7. (2pts) What is the difference between the Mealy and Moore models of sequential design?

8. (6pts) A three-variable logic function that is equal to 1 if any two or all three of its variables are equal to 1 is called a majority function. Design a minimum-cost circuit that implements this majority function.

9. (9pts) We know that a single cell of a ripple carry adder implements the functions

$Cout = AB + AC_{in} + BC_{in}$

and

$Sum = A \text{ xor } B \text{ xor } Cin$

Assuming you have made a 3-bit ripple carry adder using these cells, what is the worst case path through the adder? In other words, how long does it take for the answer to be correct in all cases? (I suggest you draw the circuit in order to make doing this problem easier). Use the following delay values, and assume all input signals become valid at time 0:

2-input AND:	6 ns	2-input OR:	4 ns	2-input XOR:	7 ns
3-input AND:	7 ns	3-input OR:	5 ns	3-input XOR:	11 ns

10. (6 pts) Assume you have 12-bit data words, and your memory system supports Single Error Correction. For each of the following patterns recieved from memory identify and correct any errors that may have occurred during transmission or storage. Assume the same organization of carry and data bits as we used in class. The first one is done for you.

Given: **0 0 1 0 1 0 1 1 0 0 1 0 1 0 1 1 0** The Data Word is: **010101101011**

Given: **1 1 1 0 0 1 0 0 1 0 0 1 1 0 0 1 0** The Data Word is:

11. (4 pts) You have derived the following karnaugh maps for the inputs to a JK flip-flop. Unfortunately, the parts department just called and your company is completely out of JK flip-flops. All they have left in stock is D flip-flops, which you will have to use instead. Show the resulting karnaugh map for the modified version of the circuit (the one that uses the D instead of the JK flip-flop.)

J’

			X	X	
	1	**1**	**d**	**1**	
	d	**d**	**d**	**d**	Y3
Y2	**d**	**d**	**d**	**d**	Y3
Y2	**1**				
		Y1	Y1		

K’

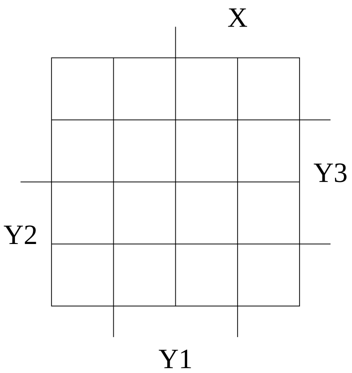
			X	X	
	d	**d**	**d**	**d**	
		1			Y3
Y2			**1**	**1**	Y3
Y2	**d**	**d**	**d**	**d**	
		Y1	Y1		

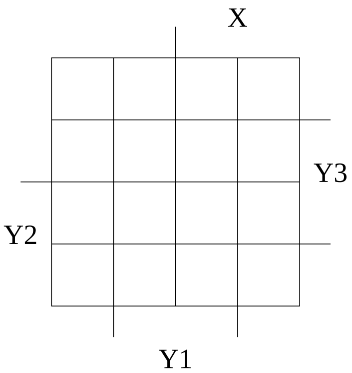
D’

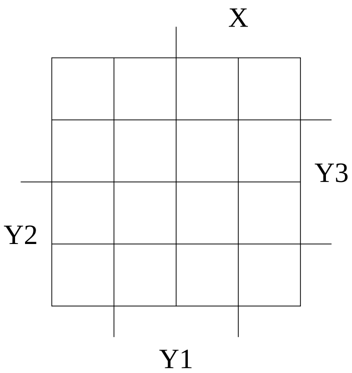
			X	X	
					Y3
Y2					Y3
Y2					
		Y1	Y1		

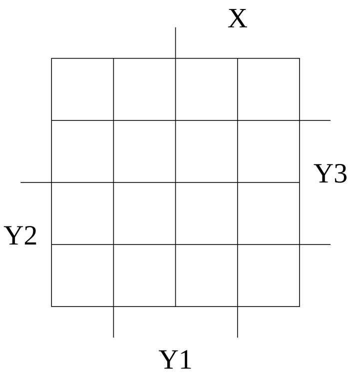
12. (20pts) Given the following table, draw the Karnaugh maps for Y1’, Y2’, and Y3’ and Z in terms of X, Y1, Y2 and Y3, and then write **minimum** boolean equations for each.

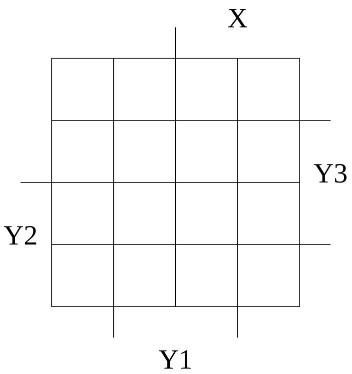
Present State (Y1 Y2 Y3)	Next State X=0 (Y1’ Y2’ Y3’)	Next State X=1 (Y1’ Y2’ Y3’)	Output (Z) X=0	Output (Z) X=1
0 0 1	0 1 1	0 1 1	1	0
0 1 0	1 0 1	1 0 1	0	0
0 1 1	1 1 1	1 1 1	1	1
1 0 0	1 0 0	1 1 0	0	0
1 0 1	0 0 0	0 1 0	1	0
1 1 0	0 0 1	0 1 0	0	1
1 1 1	1 0 1	1 1 1	1	1

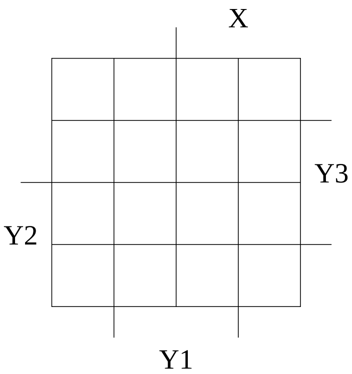












13. (20 pts) Given the following Karnaugh maps, implement the sequential machine using an SR FF for Y1, a JK FF for Y2, and a Toggle FF for Y3. You do not need to draw the gates, but you do need to write down minimized input equations for each of the inputs of each of the Flip Flops in the circuit.

Y1'

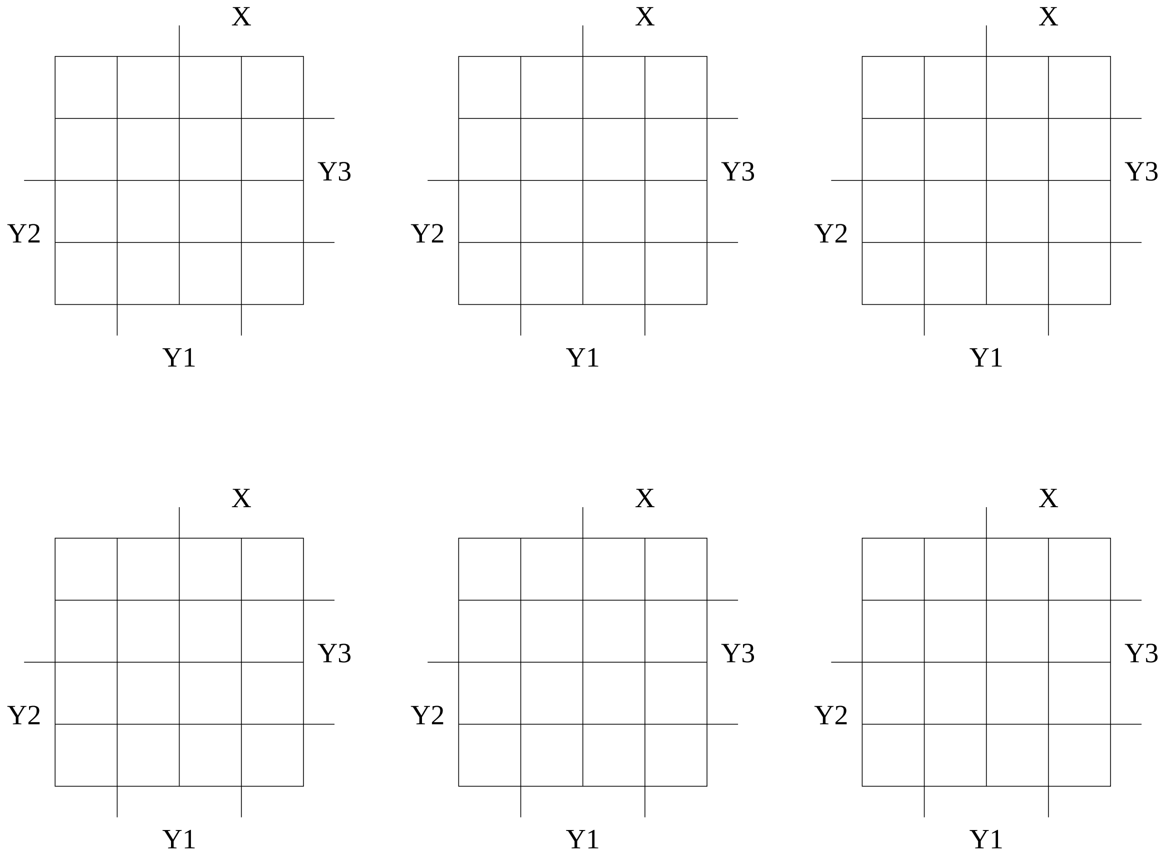
		Y1	Y1 X	X
	1			1
Y3	**1**	1	1	d
Y2 Y3	1	d		1
Y2		1	1	

Y2'

		Y1	Y1 X	X
	d		**1**	
Y3	1	d	1	1
Y2 Y3			d	
Y2	1	1	1	1

Y3'

		Y1	Y1 X	X
	1			1
Y3		1	1	
Y2 Y3		1	1	
Y2	1			1



14. (20 pts) You have been hired by the country of Freedonia to design a toll both for their national highway. In Freedonia there are only two types of coins, the 25 Somolian piece and the 15 Somolian piece. The toll booth requires an input of at least 44 Somolians before the toll gate is raised, and gives no change. Only one coin can be deposited at a time. Let X1=25 Somolians and X2=15 Somolains. Z=1 indicates the Gate should be raised, Z=0 signals No Go Joe. (Everyone in Freedonia is named "Joe", which can be *real* confusing at times ...)

Draw the State Transistion Diagram (the circles and the arcs) for this finite state machine. Let S0=nothing deposited (the Start state). Once you have a state transition diagram, minimize the number of states necessary and then assign bit patterns to each state and write down the corresponding state transition table. Assume you are using a Mealy model. Label the transitions on the diagram using the following format:

$$\frac{X1\;X2}{Z}$$

So, for example,

$$\frac{0\;1}{0}$$

would be used to indicate that a 15 Somolian piece was deposited, and the output at that point should be a 0.