Design of the PowerPC 604e™ RISC Microprocessor

Marvin Denman
Somerset Design Center

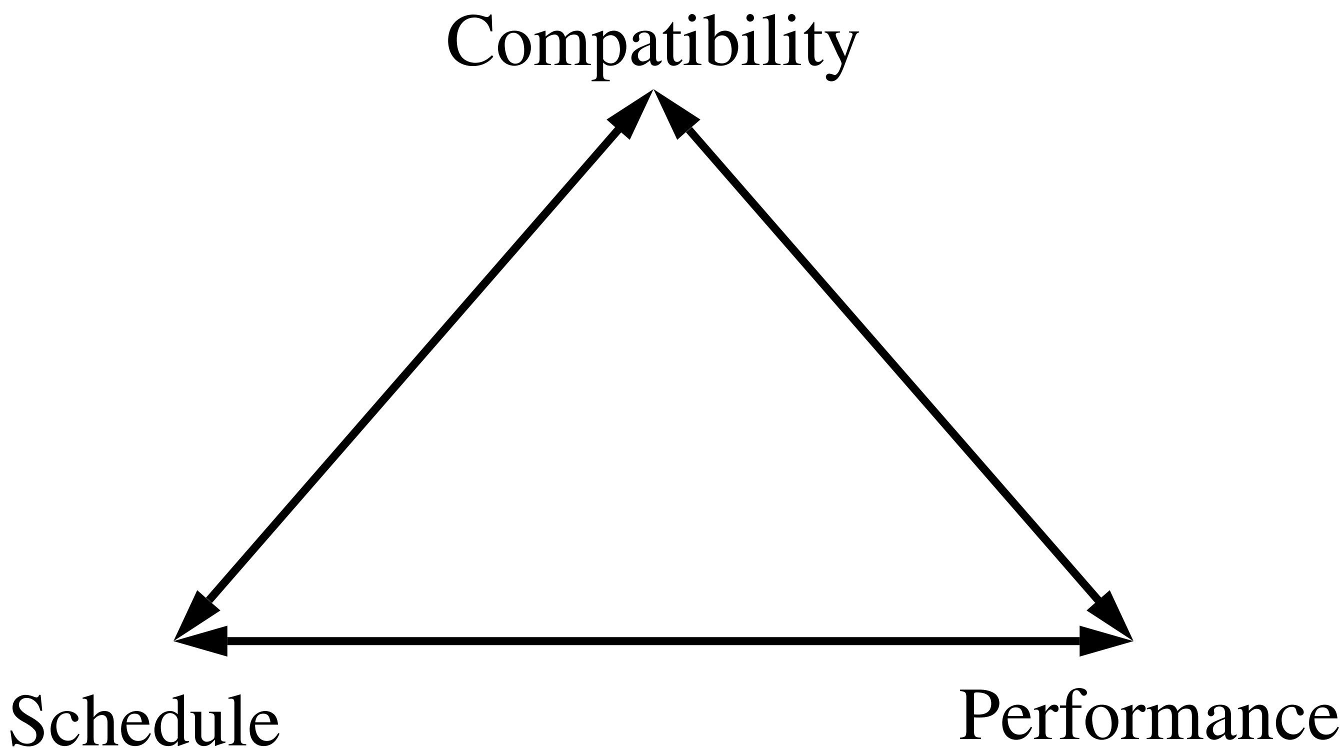
Presentation Outline

- Overview
- Execution
- Branch Prediction
- Memory System
- Summary

Overview

- Enhanced version of PowerPC 604™ micro-processor
- PowerPC™ 32-bit architecture
- Four-way superscalar
- Speculative execution
- Multiprocessor Support
- Estimated performance @ 166 Mhz
  - 6 SPECint95™
  - 5.5 SPECfp95™
- 148 mm^2, 0.35 um CMOS, 5 layer metal
- 5.6 Million transistors

Design Priorities



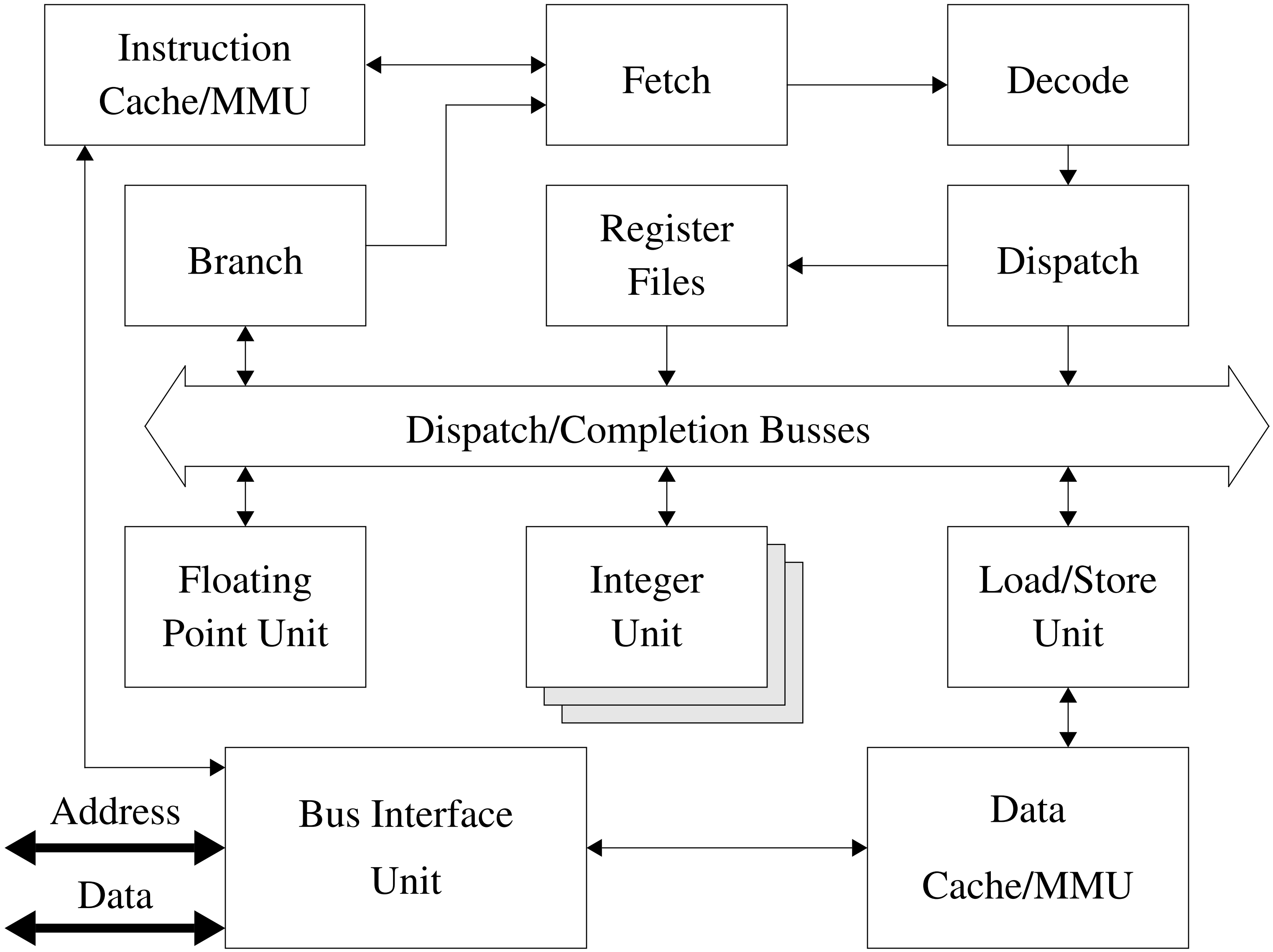
Enhancements

- 32 KB instruction and 32 KB data caches with parity
- Little endian misaligned support
- Linefill buffer forwarding
- Bus clock ratios (5:2 and 4:1)
- No DRTRY mode
- Performance monitor enhanced
- Branch enhancements

Performance Strategy

- Dynamic branch prediction
- Speculative execution with rapid correction
- Register renaming to remove false dependencies
- Reservation stations for each execution unit
- Execution serialization for non-renamed resources
- Load and store queues

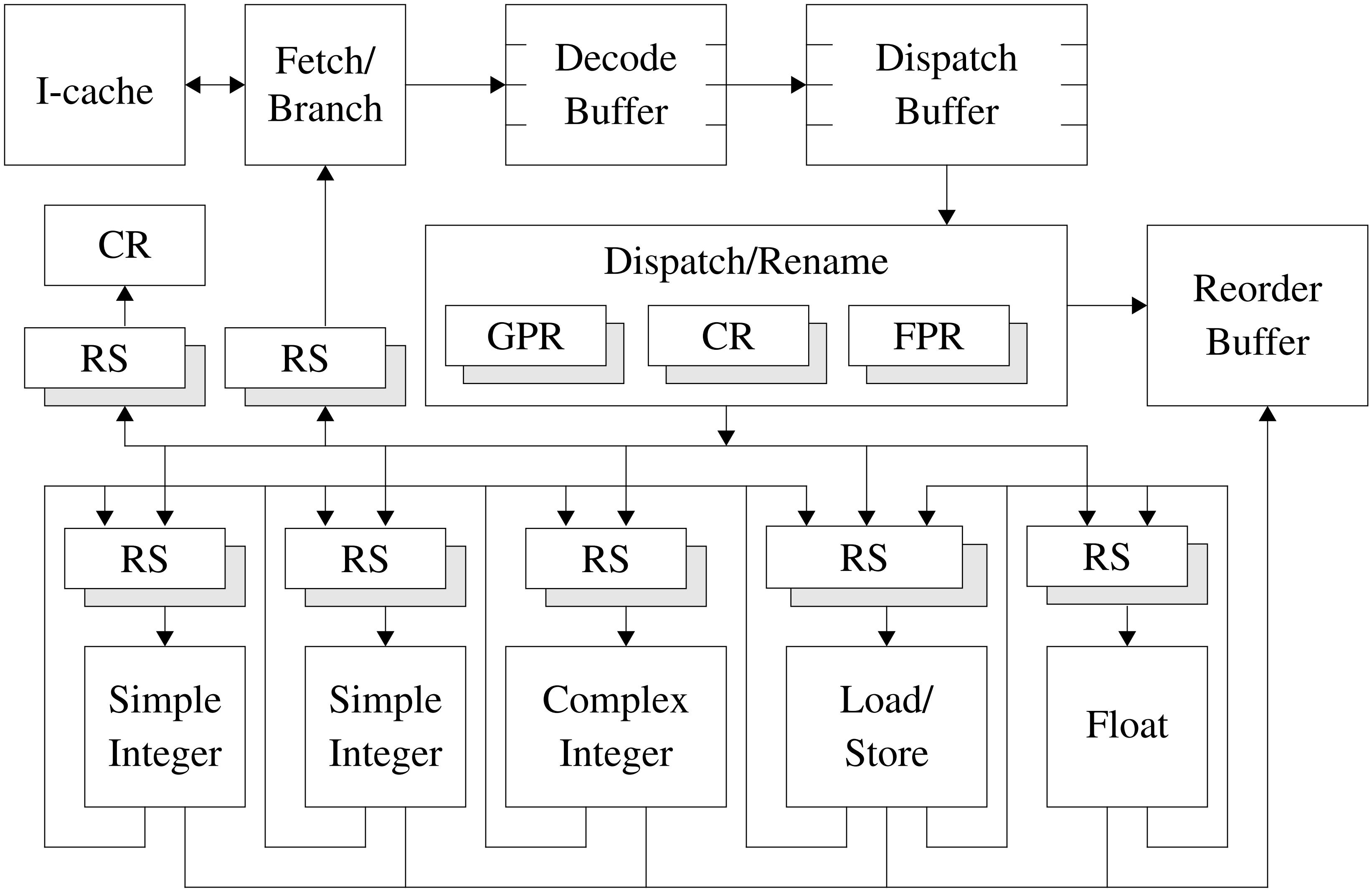
PowerPC 604e Microprocessor Block Diagram



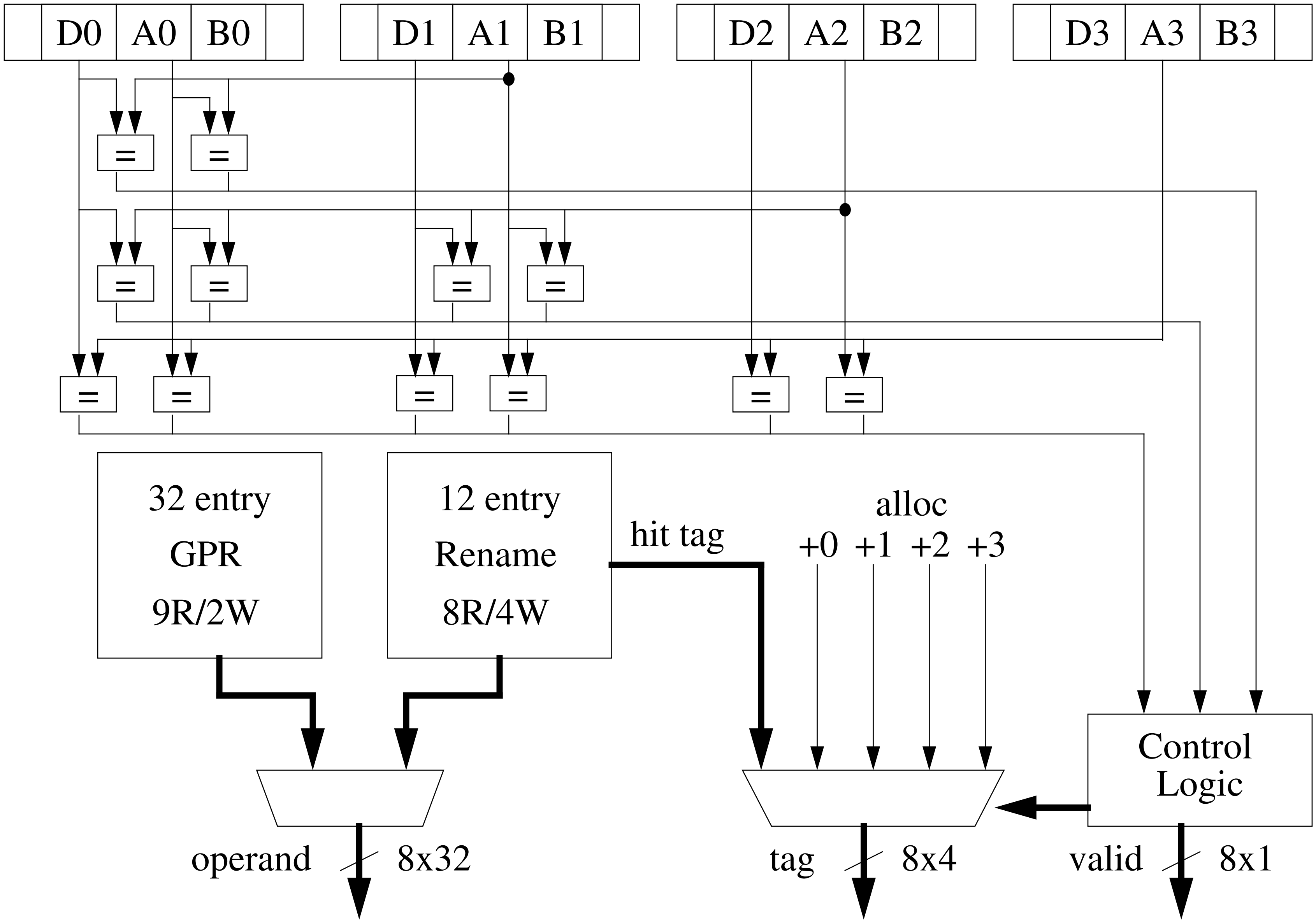
Superscalar Speculative Execution Highlights

- 6 stage pipeline
  Fetch, decode, dispatch, execute, complete, writeback
- 8-entry instruction buffer (4 decode, 4 dispatch)
- Rename registers: 12 GPR, 8 FPR, 8 CR
- 16-entry reorder buffer
- 7 execution units
- 2-entry reservation stations on each execution unit
- Fast branch misprediction recovery

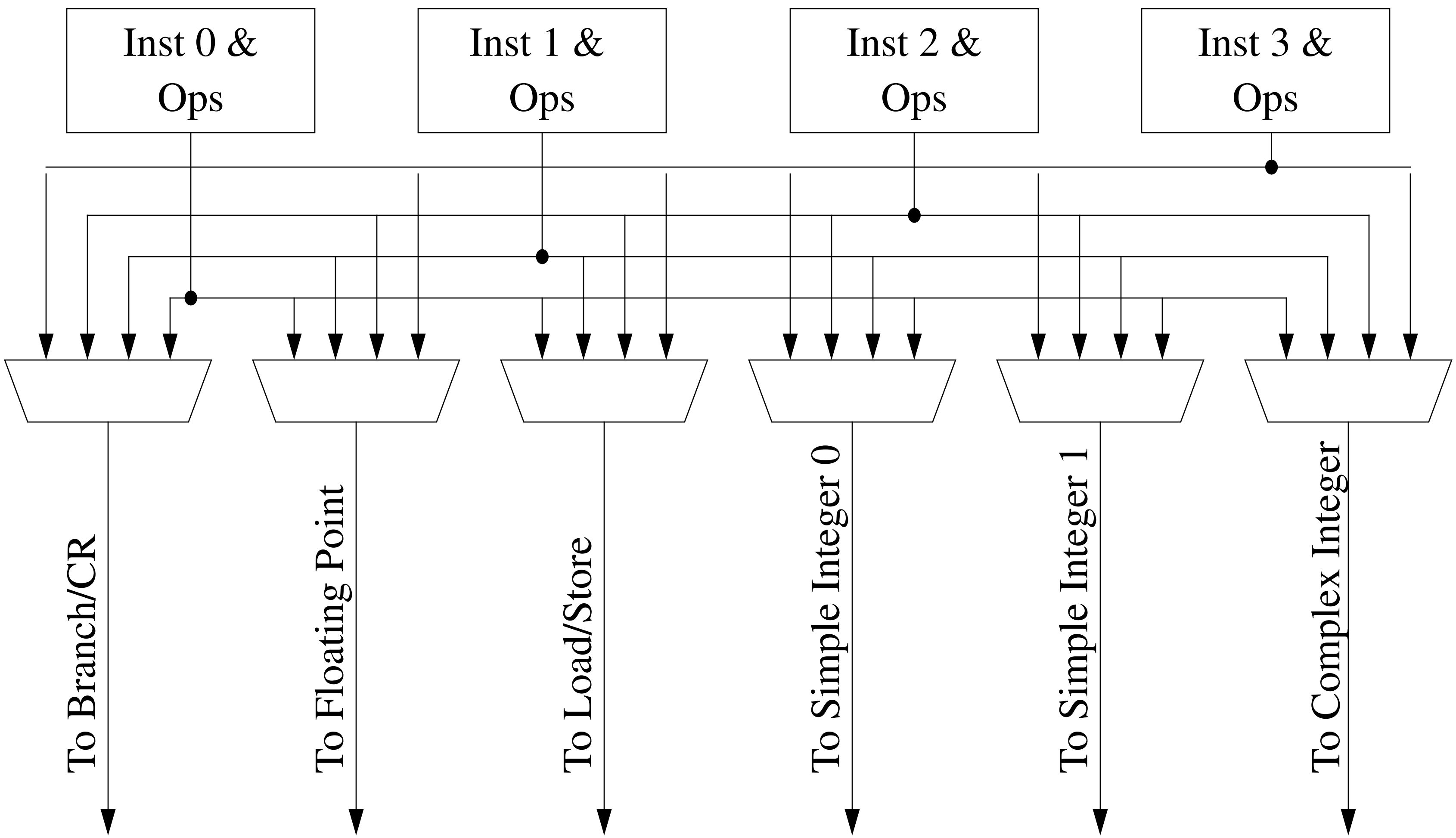
Execution


I-cache
Fetch/ Branch
Decode Buffer
Dispatch Buffer
CR
Dispatch/Rename
GPR
CR
FPR
Reorder Buffer
RS
RS
RS
RS
RS
RS
RS
Simple Integer
Simple Integer
Complex Integer
Load/ Store
Float

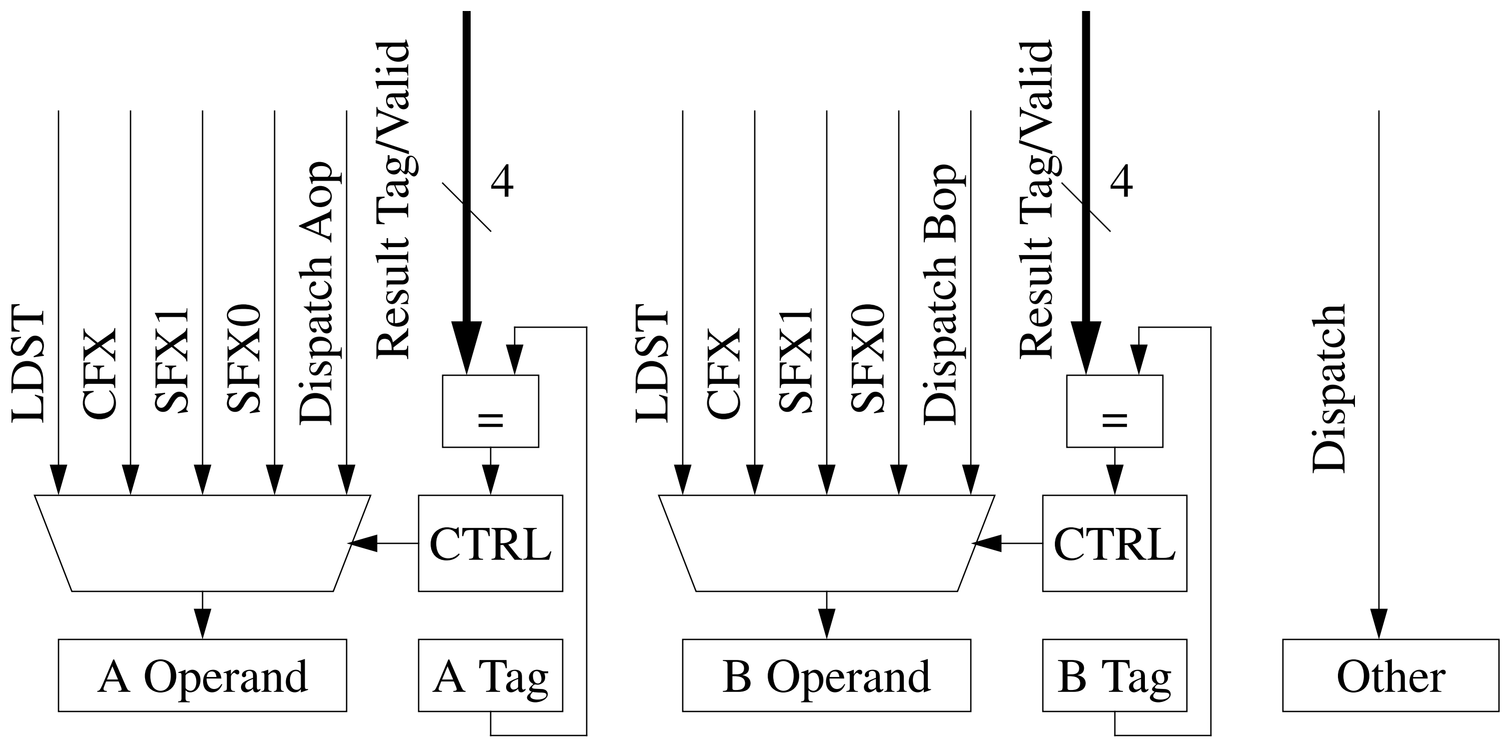
Integer RA Operand Fetch



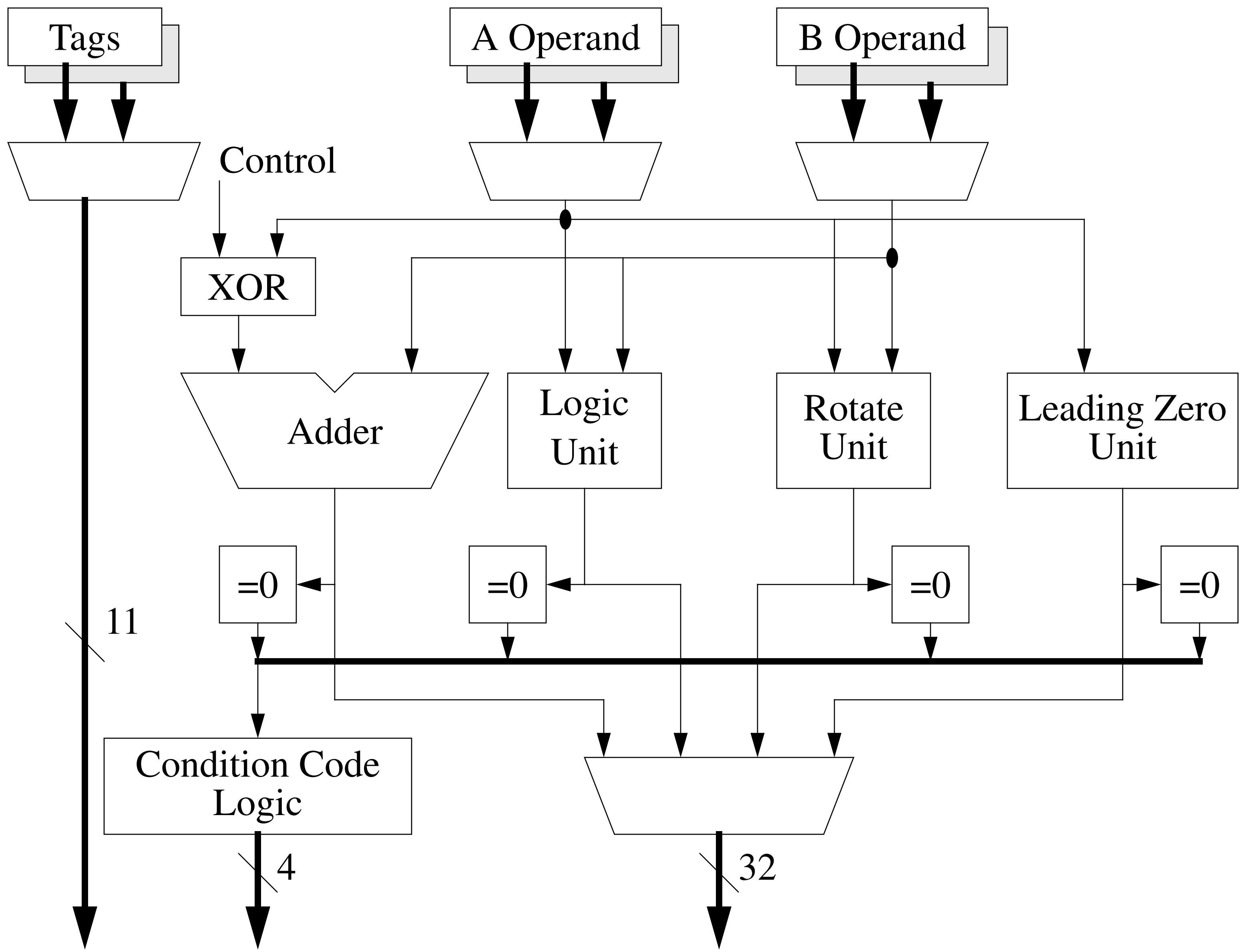
Instruction Crossbar Routing



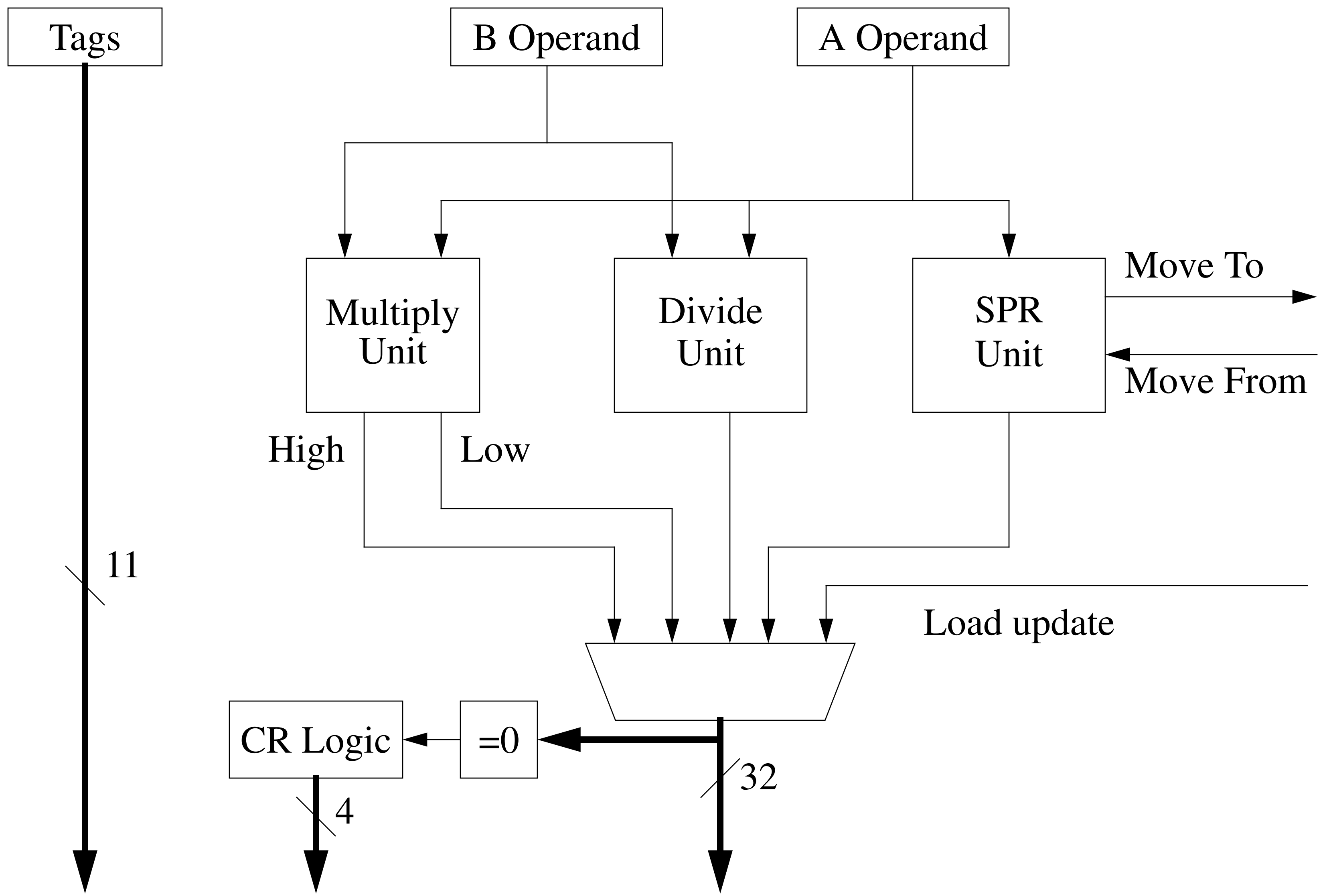
Reservation Station Entry



Simple Integer Unit



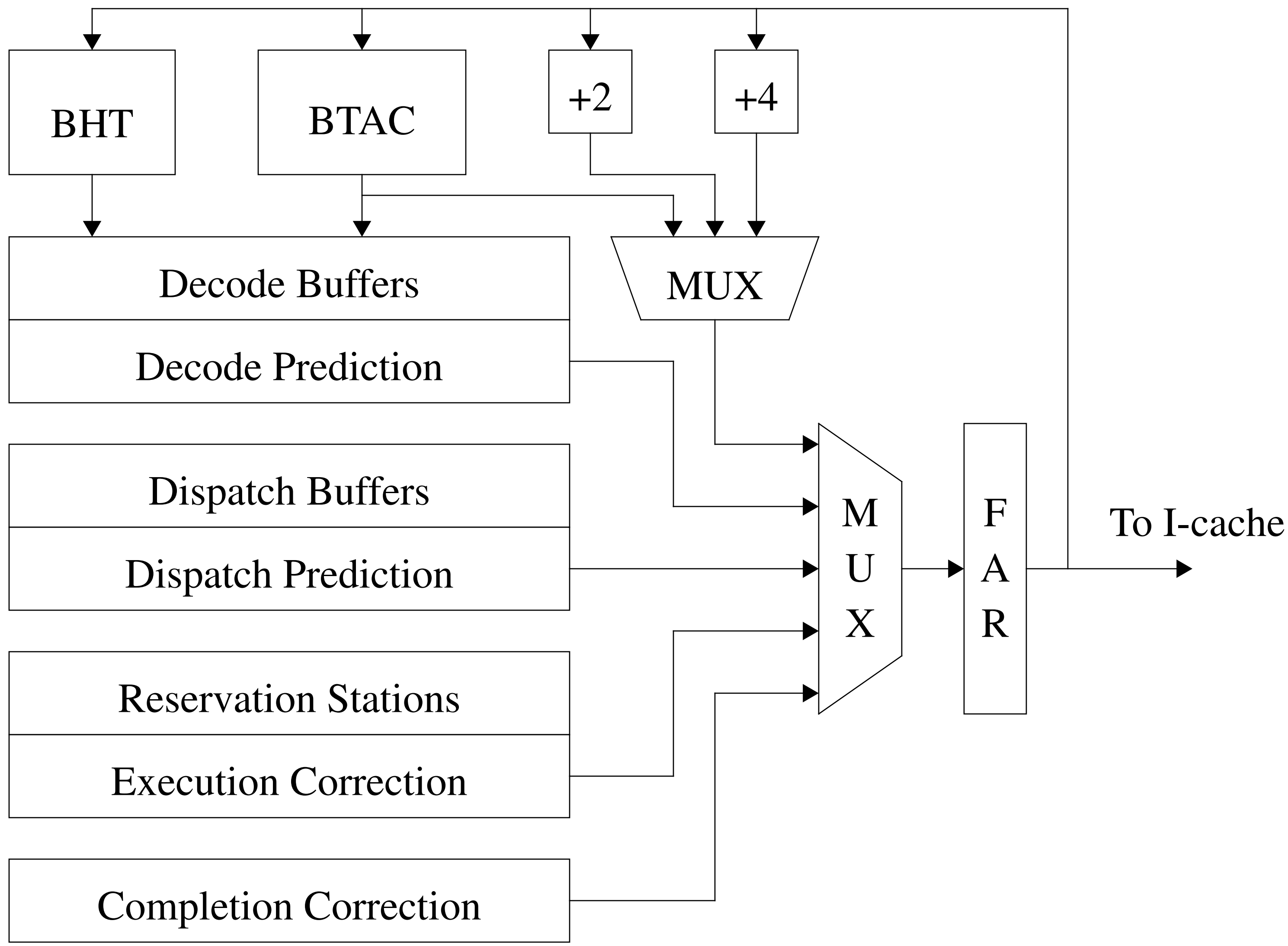
Complex Integer Unit



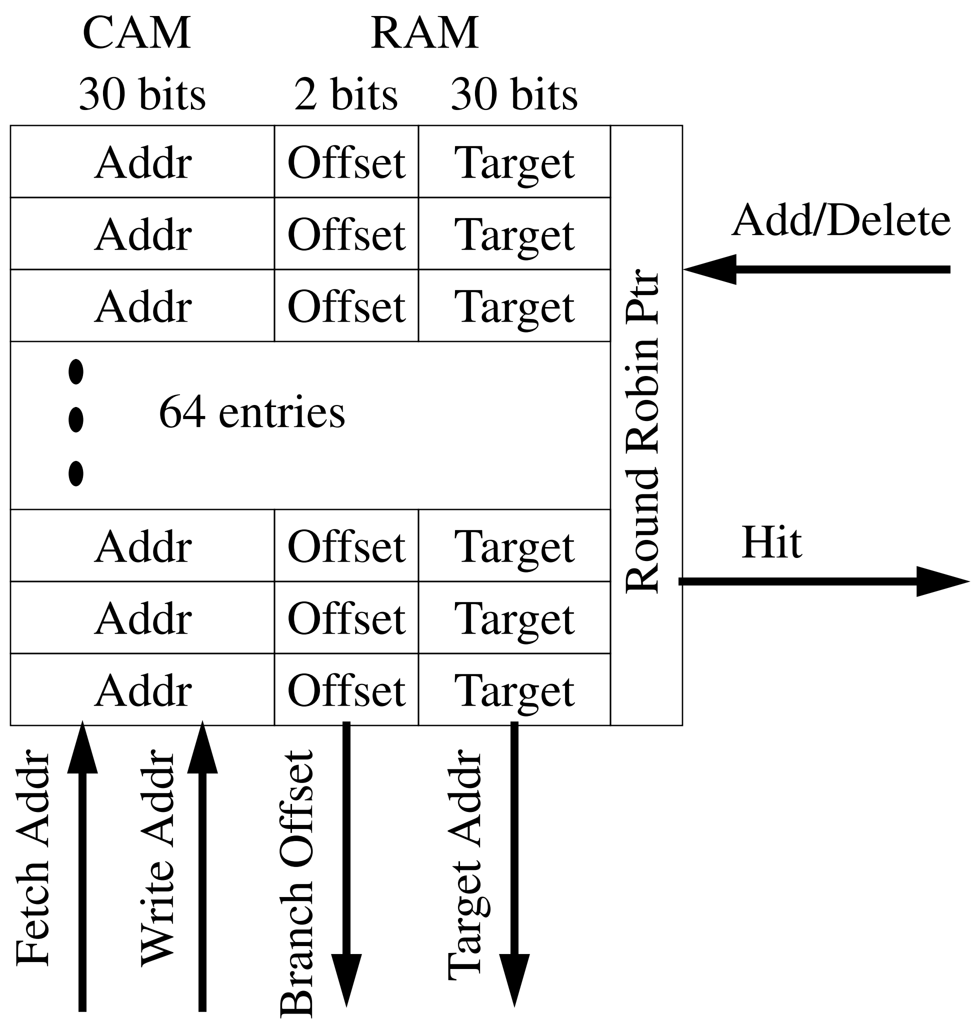
Branch Prediction Highlights

- 64-entry fully associative Branch Target Address Cache (BTAC)
- 512-entry 4-state Branch History Table (BHT)
- Prediction at fetch, decode, and dispatch stages
- Rapid misprediction correction
- Speculative execution past up to 2 branches
- Speculative fetching past up to 6 branches

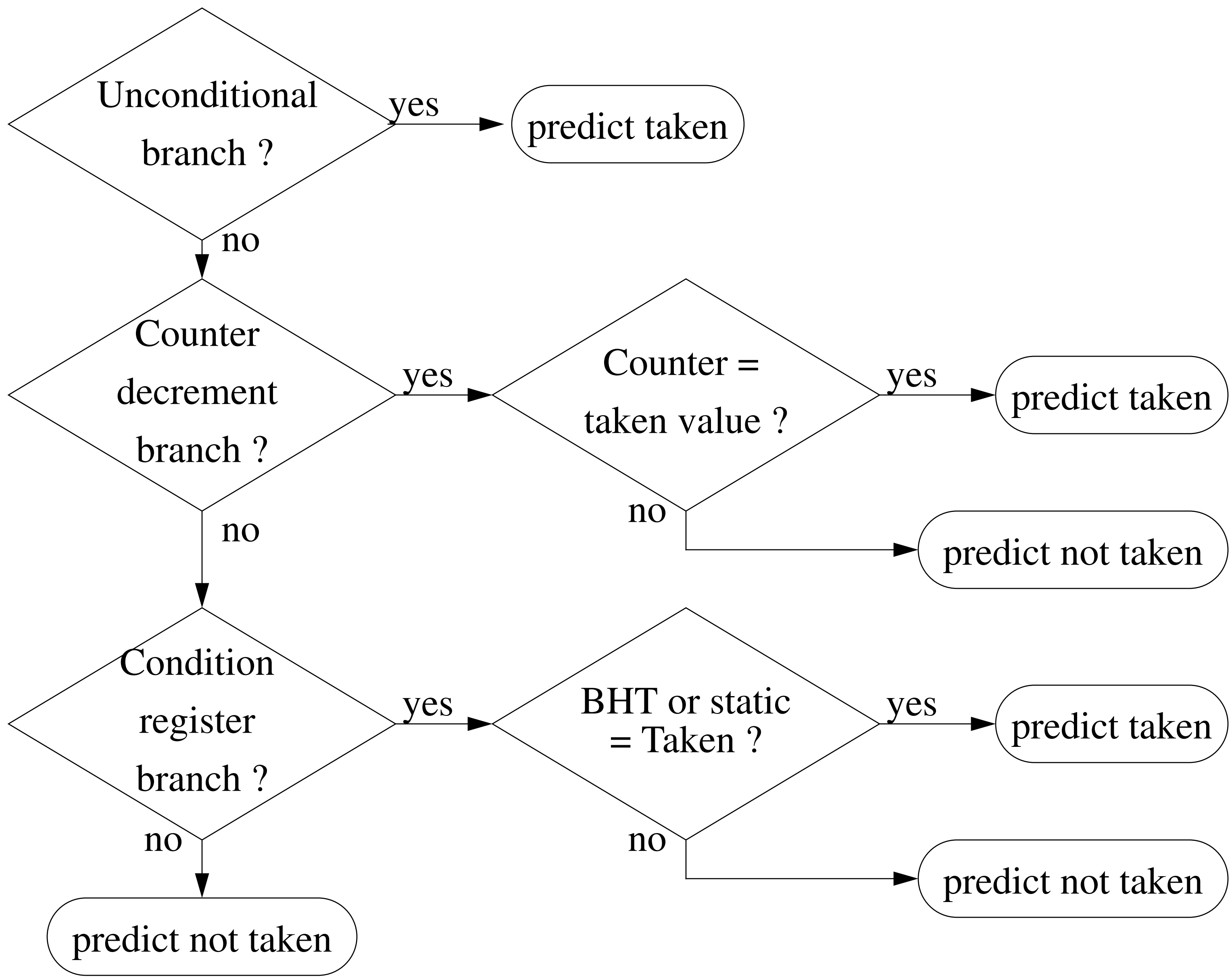
Branch Prediction Organization



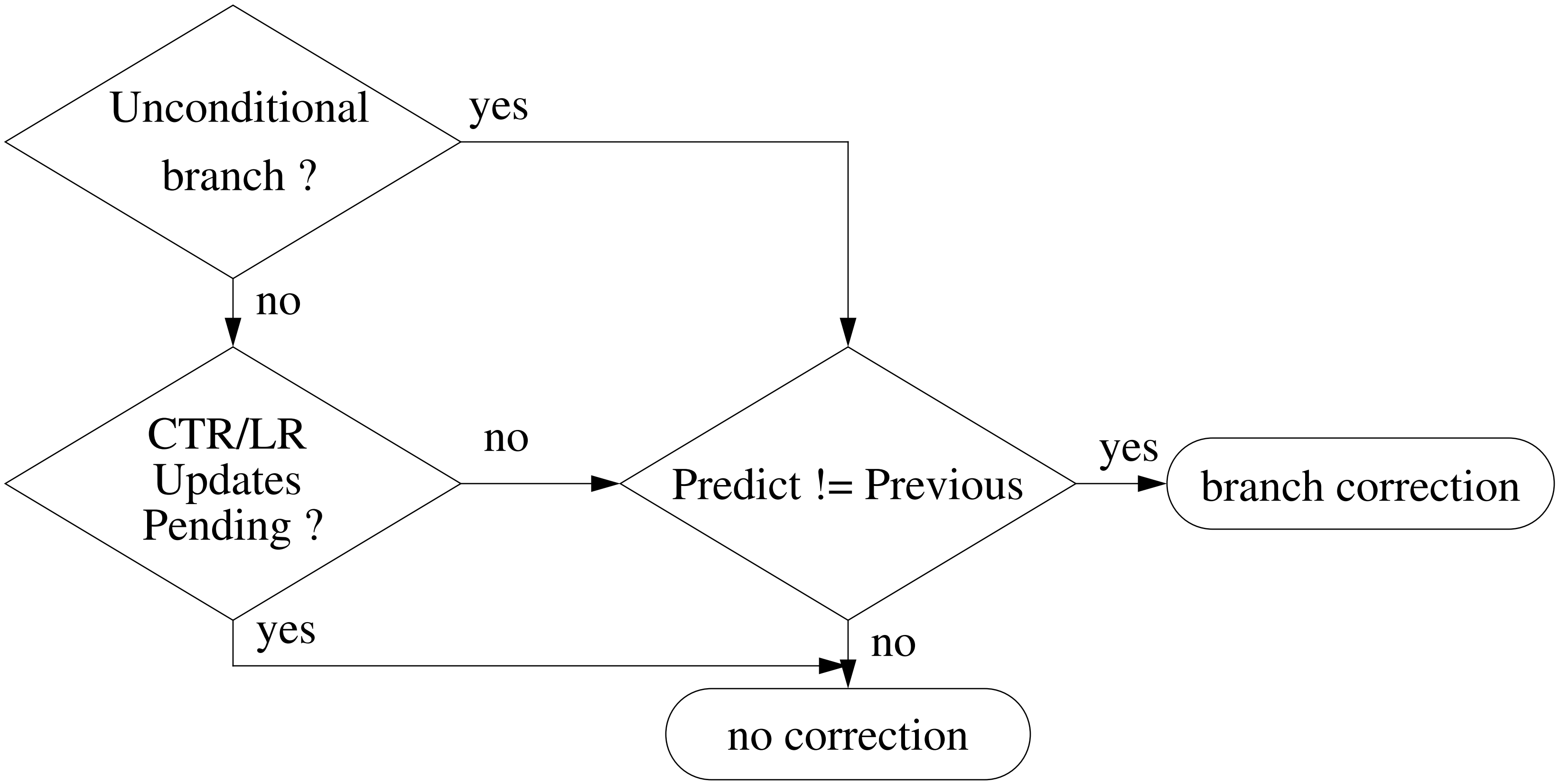
BTAC Organization



Branch Decode Prediction Logic



Branch Decode Correction Logic



NOTE: If either instruction 4 or 5 requests correction it will be done with 4 having priority.

Branch Dispatch Prediction/Correction Logic

- Prediction is same as the decode stage except:

  If the first branch/CR logical is not dispatched, we use the CR bit we read during the next cycle.

- Correction is same as the decode stage except:

  Only the first branch/CR logical can be corrected.

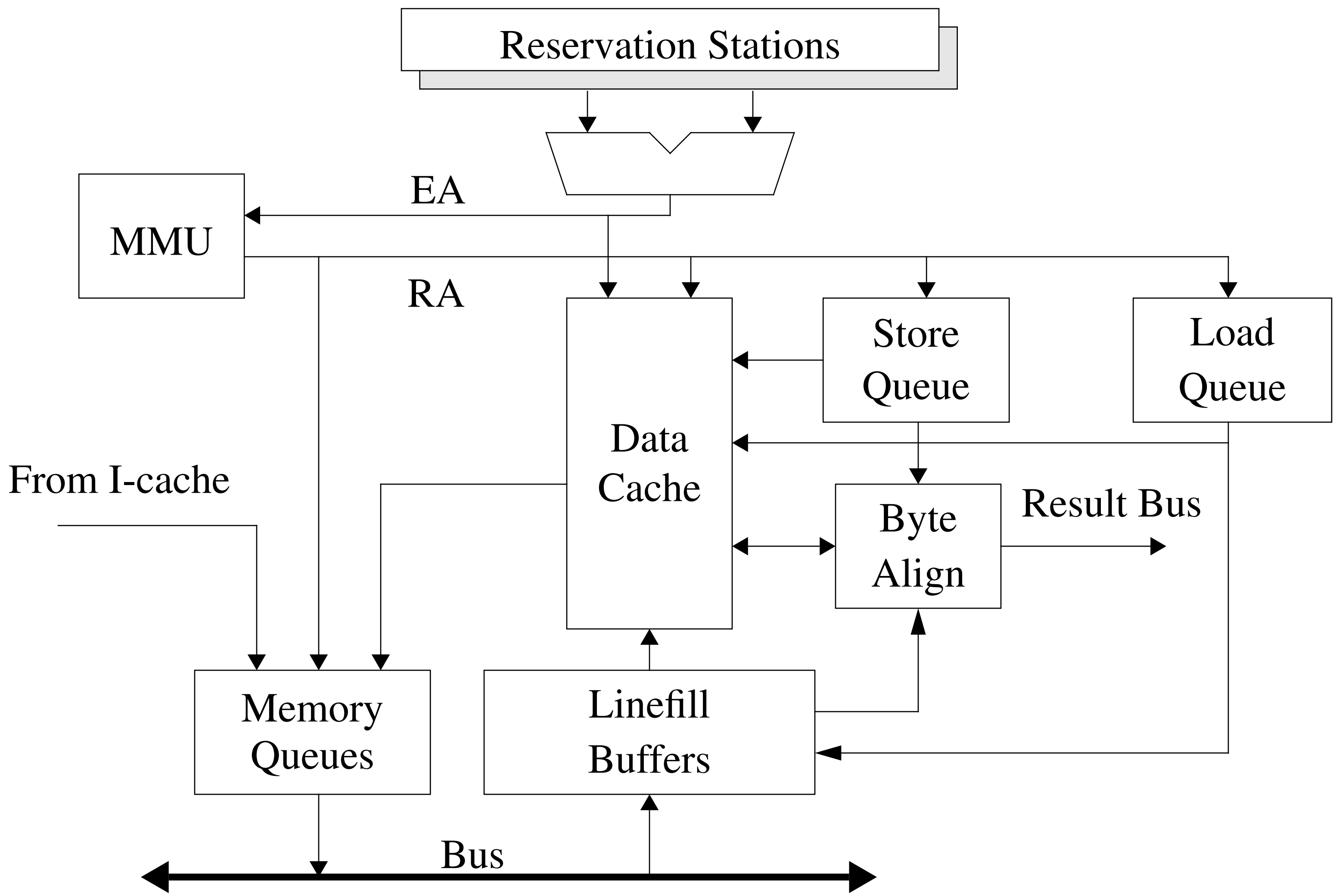
Branch Execution

- Final resolution of branches
  - Correct if wrong direction or wrong target address
- BHT update (if needed)
- BTAC update (if needed)
  - Add if next decode prediction will be taken
  - Delete if next decode prediction will be not taken
- Move addresses to 2 entry finished branch queue

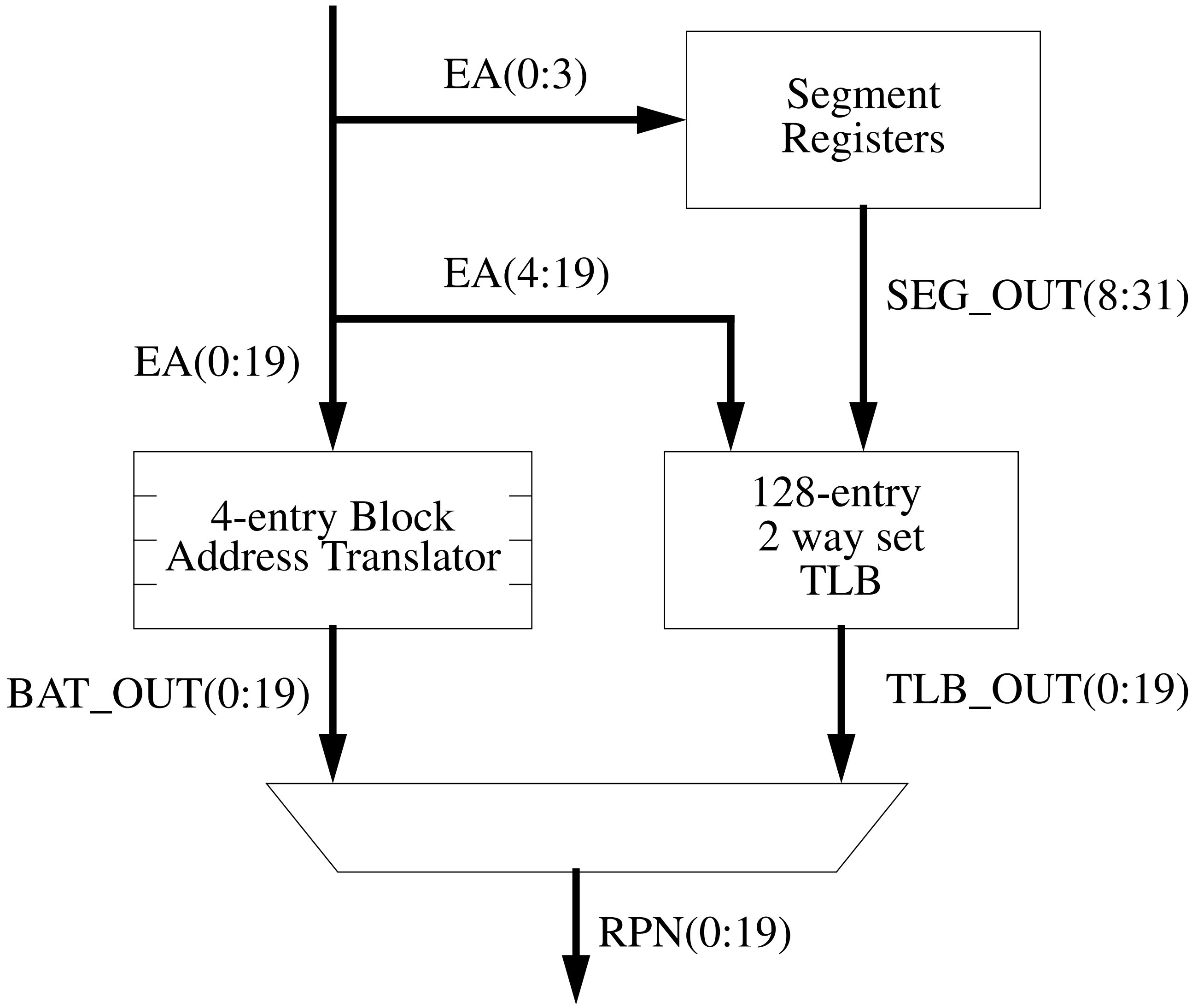
Memory Pipeline Highlights

- 32 KB instruction and 32 KB data caches with parity
- Two 128-entry two-way set associative TLBs
- Misaligned data handled in hardware (little or big endian)
- 6-entry store queue, 4-entry load queue
- 4-entry copyback queue with single cycle castout
- 2-entry data linefill buffer with forwarding
- 1-entry instruction linefill buffer with forwarding
- 2 cycle load on cache hits
- Loads can bypass stores
- Coherent data cache with copy of tags for snoop
- Caches non-blocking on misses

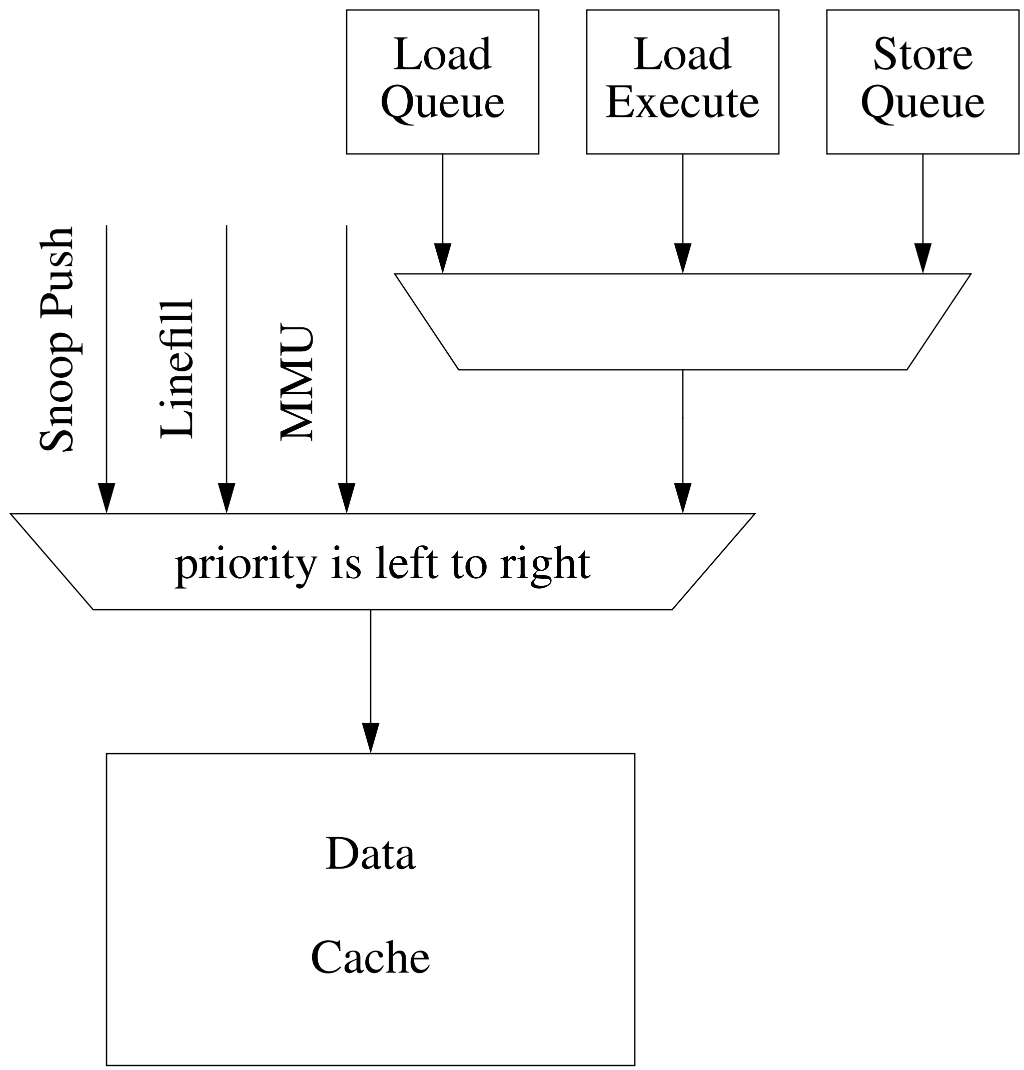
Data Memory Pipeline Organization



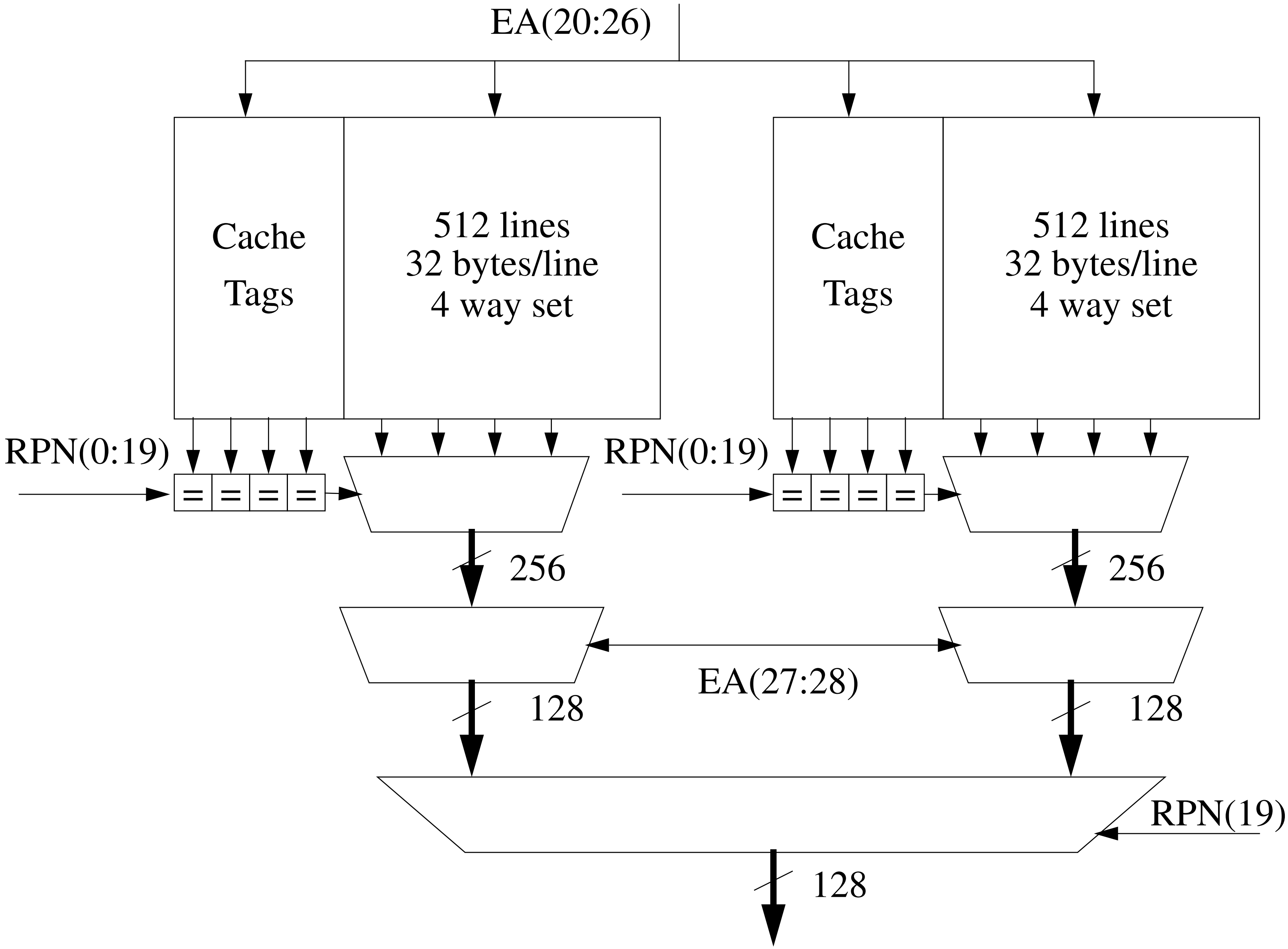
Address Translation



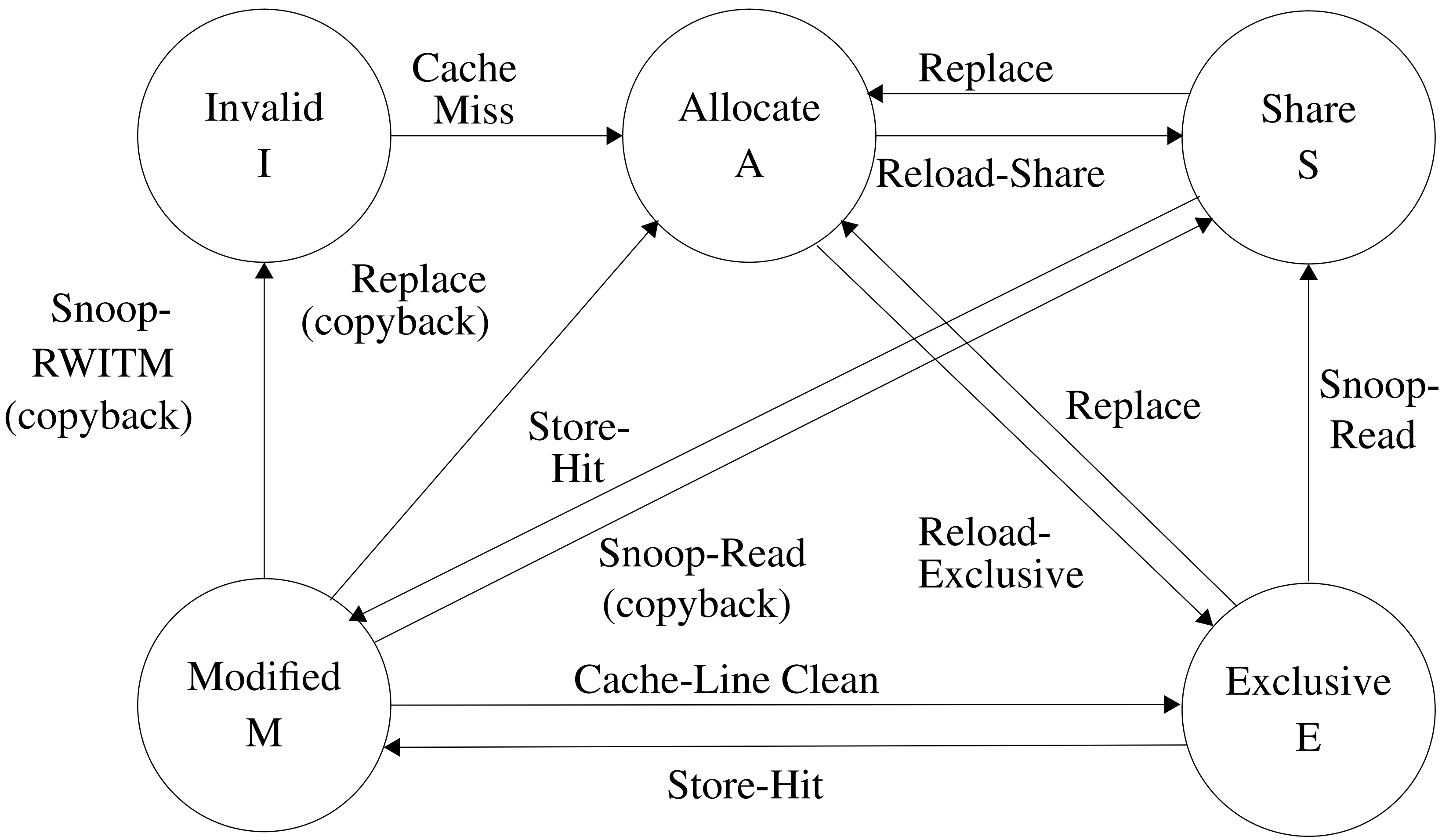
Data Cache Arbitration



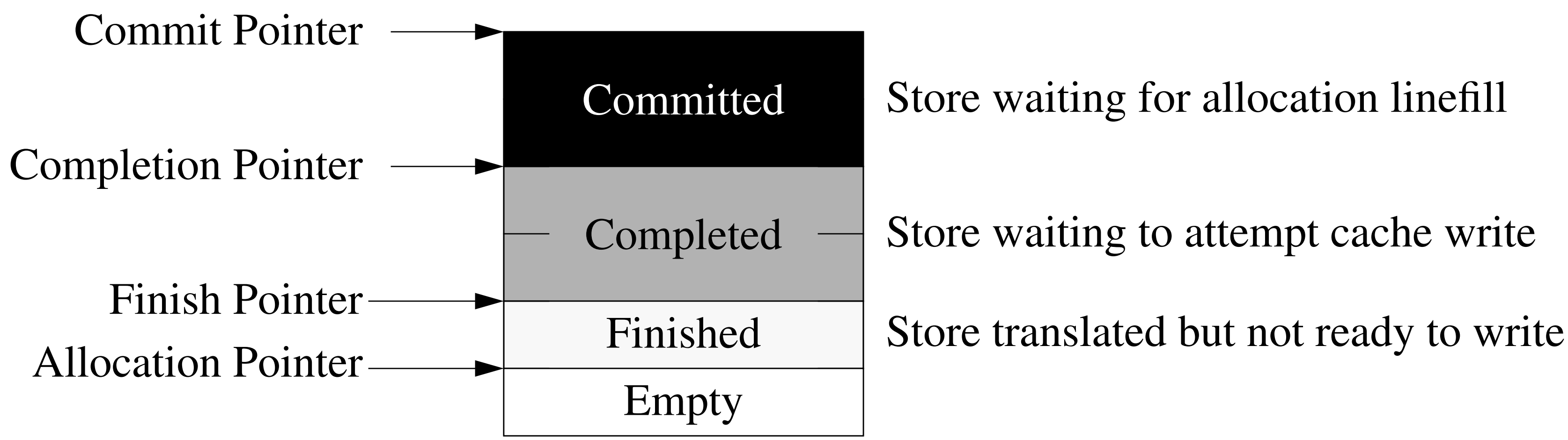
Data Cache Organization



Data Cache State Diagram
MESIA Protocol



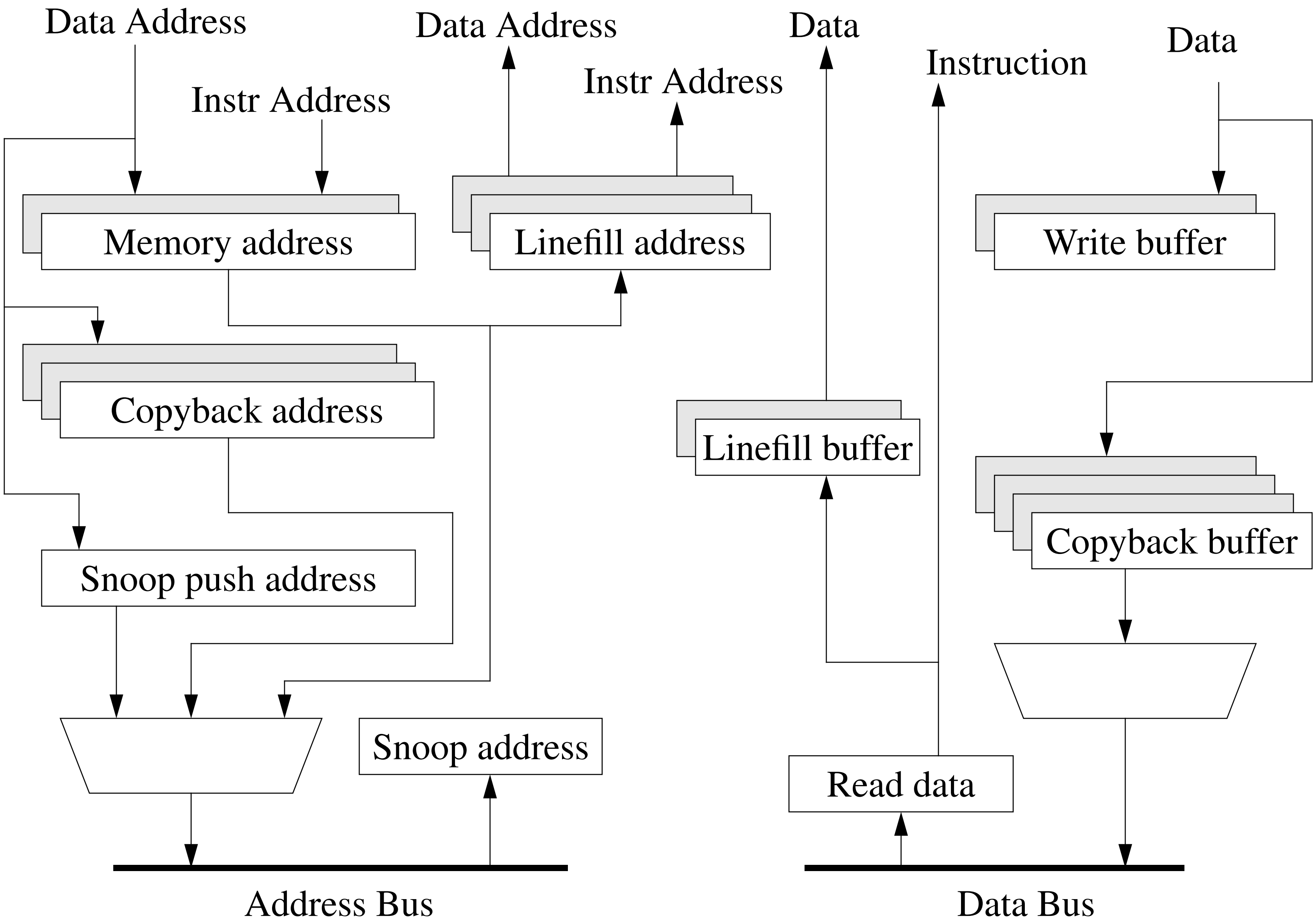
Store Queue



Store queue entry

32 bits	67 bits	38 bits
Real Addr	Data	Misc Ctrl

BIU Address and Data Queues



Performance Monitor

- ~110 different events spread over 4 counters
- Can count in user, supervisor, or both modes
- Can cause an interrupt when a counter rolls over
- Can interrupt on various timebase bits changing
- Some events can only be counted when they exceed a programmable threshhold
- Example events: instructions completed, instructions dispatched, number of cycles a unit is idle, number of entries in store queue, number of branch corrections at each stage, number of cycles dispatch is stalled for each reason

Software / System Support

- Instruction and data address breakpoints
- Single step trace and branch trace
- IEEE 1149.1 JTAG
- Nap mode that continues to snoop

Summary

- PowerPC^{TM} architecture
- 4-way superscalar processor
- Speculative execution
- 7 execution units
- Non-blocking pipelines
- Efficient memory operations
- Performance monitor
- System support

Trademarks

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