ADVANCED PROGRAM

MICRO-27

THE 27th ANNUAL IEEE/ACM
INTERNATIONAL SYMPOSIUM ON MICROARCHITECTURE

with special emphasis on
Instruction-Level Parallel Processing

San Jose, California
November 30 - December 2, 1994

Sponsored by **IEEE TC-MICRO** and **ACM SIGMICRO**

On behalf of the entire organizing committee, it is my pleasure to invite you to the 27th Annual International Symposium on Microarchitecture being held this year in in San Jose, California from November 30 - December 2, 1994.

For the past 26 years, the annual MICRO conference has provided a key venue for the dissemination of ideas and advances in the field of computer microarchitecture research. MICRO has recently become the premier forum for discussing and debating issues relating to instruction-level parallelism; and I am pleased to report that this trend has continued this year. We received a substantial number of outstanding submissions, each of which was rigorously reviewed by at least 4 qualified individuals (both program committee members and outside reviewers). Based on these reviews, the program committee has put together a strong program covering all facets of high-performance CPU design and compilation.

In addition to the paper presentations, Micro'27 will feature four invited lectures. These presentations will cover micro-architecture topics ranging from commercial state of the art microprocessors to supercomputing, and alternative ways of looking at high-performance CPUs. In particular, I would like to thank Wen-mei Hwu for agreeing to give the keynote speech. His visions will be of great interest in their own right.

After a long time the Micro conference has returned to Silicon Valley. San Jose has been selected as the host city because of its proximity to many of the valley's industries and universities, its many local attractions, and the cities and attractions of the greater San Francisco and Monterey Bay areas.

In addition to the excellent slate of presentations, MICRO is famous for it's opportunities for personal interaction with leading researchers in the area. I invite you to join us in San Jose, and I look forward to personally greeting each and every one of you!

Hans Mulder General Chair

The Program
Wednesday, November 30

8:30- 9:00 Welcoming Remarks: Hans Mulder, Gen Chair

9:00-10:00 Kenote Address: Wen-Mei Hwu, Illinois
Title: "VLIW: is it for real this time?"

10:00-10:30 Break

10:30-12:00 Session 1: Branch Profiling and Classification

"Static Branch Frequency and Program Profile Analysis"
Youfeng Wu - Sequent Computer Systems, James R. Larus - Wisconsin (USA)

"Using Branch Handling Hardware to Support Profile-Driven Optimization"
Thomas M. Conte, Burzin A. Patel - South Carolina, J. Stan Cox - AT&T (USA)

"Branch Classification: A New Mechanism for Improving Branch Predictor Performance"
Po-Yung Chang, Yale Patt - University of Michigan, Ann Arbor (USA)

12:00-1:30 Lunch (on your own)

1:30-3:00 Session 2: Random Acts of Research

"Techniques for Compressing Program Address Traces"
Andrew Pleszkun - University of Colorado, Boulder (USA)

"Height Reduction of Control Recurrences for ILP Processors"
Michael Schlansker, Vinod Kathail, Sadun Anik - HP Labs (USA)

"Theoretical Modeling of Superscalar Processor Performance"
Derek B. Noonburg, John P. Shen - Carnegie Mellon University (USA)

3:00-3:30 Break

3:30-5:20 Session 3: Software Pipelining and ILP Scheduling

"Iterative Modulo Scheduling: An Algorithm For Software Pipelining Loops"
B. Ramakrishna Rau - HP Labs (USA)

"Minimum Register Requirements for a Modulo Schedule"
Alexandre E. Eichenberger, Edward S. Davidson - University of Michigan, Ann Arbor, Santosh G. Abraham - HP Labs (USA)

"Minimizing Register Requirements under Resource-Constrained Rate-Optimal Software Pipelining"
R. Govindarajan - Newfoundland, Erik R. Altman, Guang R. Gao - McGill (CANADA)

"Software Pipelining with Register Allocation and Spilling"
Jian Wang, Andreas Krall, M. Anton Ertl - Technische Universitat Wein (AUSTRIA), Christine Eisenbeis - INRIA (FRANCE)

6:30- 8:00 Welcoming Reception

8:00-10:00 Business Meeting

Thursday, December 1

9:30-10:30 Session 4: Memory Disambiguation

"Reducing Memory Traffic with CRegs"
Peter Dahl, Matthew O'Keefe - University of Minnesota (USA)

"Dynamic Memory Disambiguation for Array References"
David Bernstein, Doron Cohen - IBM (ISRAEL), Dror E. Maydan - SGI (USA)

"A Study of Pointer Aliasing for Software Pipelining using Run-time Disambiguation"
Bogong Su, Stanley Habib - CUNY, Wei Zhao - Case Western (USA), Jian Wang - Technische Universitat Wein (AUSTRIA), Youfeng Wu - Sequent

---

10:30-11:00 Break

11:00-12:00 Session 5: Memory System Optimizations

"Data Relocation and Prefetching for Programs with Large Data Sets"
Yoji Yamada, John Gyllenhaal, Grant Haab, Wen-mei Hwu - University of Illinois, Urbana (USA)

"Cache Designs with Partial Address Matching"
Lishing Liu

12:00-1:30 Lunch (on your own)

1:30-3:00 Session 6: Hardware Evaluation and Analysis

"Minimizing Branch Misprediction Penalties for Superpipelined Processors"
Ching-Long Su, Alvin M. Despain - USC (USA)

"Facilitating Superscalar Processing via a Combined Static/Dynamic Register Renaming Scheme"
Eric Sprangle, Yale Patt - University of Michigan, Ann Arbor (USA)

"Improving Resource Utilization of the MIPS R8000 via Post-Scheduling Global Instruction Distribution"
Raymond Lo, Sun Chan, Fred Chow, Shin-Ming Liu - MIPS Technologies (USA)

"A Comparison of Two Pipeline Organizations"
Michael Golden, Trevor Mudge - University of Michigan, Ann Arbor (USA)

3:00-3:30 Break

3:30-5:20 Session 7: Hardware Design

"A Fill-Unit Approach to Multiple Instruction Issue"
Manoj Franklin, Mark Smotherman - Clemson University (USA)

"A High-Performance Microarchitecture with Hardware-Programmable Functional Units"
Rahul Razdan - DEC (USA), Michael D. Smith - Harvard University (USA)

"The Anatomy of the Register File in a Multiscalar Processor"
Scott E. Breach, T. N. Vijaykumar, Gurindar S. Sohi - Wisconsin (USA)

"Register File Port Requirements of Transport Triggered Architectures"
Jan Hoogerbrugge, Henk Corporaal - Delft University (NETHERLANDS)

6:30-9:00 Conference Dinner
Invited Speaker: Steve Wallach, Convex
Title:"Toward a TeraMips future"

Friday, December 2nd

9:00-10:00 **Invited Speaker:** Kunle Olukotun, Stanford
Title:"Multiprocessor Microarchitectures: A New Direction for High Performance Computing"

10:00-10:30 **Break**

10:30-12:20 **Session 8:** **Predicated Execution and Branch Prediction**

"The Effects of Predicated Execution on Branch Prediction"
Gary Tyson - University of California, Davis (USA)

"Analysis of the Conditional Skip Instructions of the HP Precision Architecture"
Jonathan P. Vogel - Telxon Corporation (USA), Bruce K. Holmer - Northwestern University (USA)

"Characterizing the Impact of Predicated Execution on Branch Prediction"
Scott A. Mahlke, Richard E. Hank, Roger A. Bringmann, John C. Gyllenhaal, David M. Gallagher, Wen-mei W. Hwu - University if Illinois, Urbana (USA)

"The Effect of Speculatively Updating Branch History on Branch Prediction Accuracy, Revisited"
Eric Hao, Yale Patt - University of Michigan, Ann Arbor (USA)

12:20-1:45 **Conference Luncheon**

1:45-3:00 **Invited Speaker:** Leslie Kohn, SUN Microsystems
Title: "UltraSparc"

Micro-27 Organizing Committees

GENERAL CHAIR
Hans Mulder
Intel Corporation
2200 Mission College Blvd.
P. O. Box 58119, RN2-27
Santa Clara, CA 95052-8119
hmulder@mipos2.intel.com
(408) 765-5456

PROGRAM CHAIR
Matthew Farrens
Department of Computer Science
University of California, Davis
Davis, CA 95616-8562, USA
farrens@cs.ucdavis.edu
(916) 752-9678, 752-4767 FAX

LOCAL ARRANGEMENTS CHAIR
Tse-Yu Yeh, Intel

STEERING COMMITTEE
Richard Belgard, Consultant
James Bondi, Texas Instruments
Matthew Farrens, UC Davis
Wen-mei Hwu, U. Illinois
Gearold Johnson, Nat'l Technol. U.
Joe Linn, Microsoft
Yale Patt, U. Michigan
Andrew Wolfe, Princeton

PROGRAM COMMITTEE
Vicki Allan, Utah State
Richard Belgard, Consultant
David Bernstein, IBM Israel
James Bondi, Texas Instruments
Bob Colwell, Intel
Tom Conte, U. South Carolina
Henk Corporaal, Delft University
Jim Dehnert, Silicon Graphics

PROGRAM COMMITTEE (cont)
Alvin Despain, USC
Kemal Ebcioglu, IBM
Matt Farrens, UC Davis
Mike Flynn, Stanford
Stanley Habib, CUNY
Wei Hsu, Hewlett-Packard
Wen-mei Hwu, U. Illinois
Gearold Johnson, Nat'l Technol. U.
Bill Mangione-Smith, Motorola
Steve Melvin, Consultant
Trevor Mudge, Michigan
Alex Nicolau, UC Irvine
Yale Patt, U. Michigan
Andrew Pleszkun, Colorado
Jim Smith, Cray Research
Mike Smith, Harvard
Andrew Wolfe, Princeton

MICRO-27 REGISTRATION INFORMATION

Registration

Early registration must be postmarked by October 28, 1994. Full payment in U.S. dollars must accompany registration: check drawn from a U.S. bank or charge to a MasterCard or Visa card. Credit card registrations may be faxed to (408) 765-6415, attn: Jan Harper. Conference registration includes one copy of the proceedings, lunch, reception, dinner, and coffee breaks. The student registration fee does include all meals. Student registration must include a copy of a valid, full-time student ID.

Conference Site and Accomodation

All technical sessions, reception, lunch, and registration will be held at the Fairmont Hotel. Contact the hotel directly for reservation and indicate MICRO'27 conference. Conference rates are $90 per night for single or double room (10% city occupancy tax not included). Reservations must be received by November 8, 1994, to guarantee conference rate. Late reservations will be accepted on a space-available basis.

The Fairmont Hotel is conveniently located in Downtown San Jose. It is adjacent to the city's light-rail transit line and is within walking distance of theaters, museums, civic buildings, and Center of Performance Arts.

Fairmont Hotel
At Fairmont Plaza
170 South Market Street
San Jose, CA 95113-2395
1-800-527-4727 or (408) 998-1900
FAX (408) 280-0394

Ground Transportation

The Fairmont Hotel is less than 10 minutes from the San Jose International Airport. There is a complimentary shuttle service to and from the airport: Weekdays, 5:30 a.m. to 11 p.m., and Weekends, 7 a.m. to 11 p.m. Taxi fare is approximately $6 one way.

Weather

December weather in San Jose is variable. There is a chance of rain. Day-time temperatures are between 45 and 65 degrees F. Evenings and nights will be chilly.

San Jose and the Surrounding Area

For decades, visitors have used San Jose as a gateway to San Francisco 50 miles to the north, and to the Monterey Peninsula 70 miles to the south. Now, thanks to an eight-year, $1.5 billion investment to revitalize the city's downtown visitors will find plenty to do just minutes away within the San Jose metropolitan area.

Some of the most favorite attractions in and around San Jose are: the Egyptian Museum, the San Jose Historical Museum, the San Jose Museum of Art, the Tech Museum of Innovation, winery tours, and all kinds of performing arts. San Francisco is only 50 miles away and can easily be reached for day trips by train or car.

Micro'27 Registration Form

November 30 - December 2, 1994
San Jose, California

Name _____

Affiliation _____

Address _____

_____

Telephone _____

Fax _____

Electronic _____

Mail Address _____

X ACM X IEEE Member Number _____

Please list any special needs or accommodations:

_____

_____

_____

	Before Oct. 28	After Oct. 28
Member	$285	$345
Non-member	$360	$430
Student*	$200	$240

* Student registration must be accompanied by a copy of a valid, full-time student ID; also see the student travel grant program.

X Check drawn on U.S. bank payable to: **MICRO'27**
X Mastercard X Visa

Card No. _____

Expiration Date _____

Name on Card _____

Signature _____

Send or Fax registration form with payment to:

MICRO'27
c/o Jan Harper
Intel Corporation
2200 Mission College Blvd. MS RN6-16
Santa Clara, CA 95052
Fax: (408) 765-6415

A copy of this form may be retrieved by anonymous ftp from **american.cs.ucdavis.edu:/Micro27**, on the World Wide Web via Mosaic at **http://www.cs.ucdavis.edu/Micro27.html**), or by mailing **farrens@cs.ucdavis.edu**. For further information, contact Jan Harper at micro27@austin.intel.com.

STUDENT TRAVEL GRANT INFORMATION

MICRO-27

THE 27th ANNUAL INTERNATIONAL SYMPOSIUM ON MICROARCHITECTURE

I am pleased to announce the availability of MICRO-27 student travel grants. The grant program is made possible through a generous donation from Hewlett-Packard. The purpose of the grant is to supplement the advisors' research grants or the students' fellowship travel allowance to make attending MICRO-27 more affordable. The details of the grant are given below:

(1) Students who are presenting papers at MICRO-27 will be given higher priority in the selection process. We expect to have at least 30 recipients this year.

(2) We are aiming at covering approximately 50% of the airfare, hotel, and registration expenses with a maximum of $350.

(3) Student applicants should fill out the enclosed application form and e-mail the application to micro27@austin.intel.com by October 21, 1994. The receipt of the application will be acknowledged immediately. The decision will be sent to the applicants by November 1, 1994.

(4) The grant checks will be sent to the recipients AFTER the conference. Each grant recipient is required to send in a one-page summary of his/her experience with MICRO-27 after the conference via e-mail to micro27@austin.intel.com. The check will be delivered after we receive the report.

(5) The grant recipients are still required to pay the conference registration fee. Note that all student participants will be entitled to ALL MICRO-27 events and proceedings in spite of the lower registration fee for students.

Hans Mulder
Chair, MICRO-27

MICRO-27 Student Travel Grant Application Form

Name: _____

Affiliation: _____

Expected degree and graduation date: _____

Area of research: _____

Name of advisor: _____

Postal address for sending the grant check: _____

E-mail address: _____

Paper title (if presenting a paper at MICRO-27): _____

Have you published at MICRO before? If so, please list the years:

Estimate of expenses: airfare ____ hotel _____ registration _____