MATTHEW K. FARRENS

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EDUCATION

- Ph.D. in Electrical and Computer Engineering received August 1989 from the University of Wisconsin-Madison.
- M.S. in Electrical and Computer Engineering received December 1984 from the University of Wisconsin-Madison.
- B.S. in Physics and Mathematics received May 1981 from Nebraska Wesleyan University, Lincoln, Nebraska.

RESEARCH INTERESTS

- All aspects of computer architecture, but primarily in the architecture and design of high-performance single-chip processors, with a focus on how to best use a limited number of resources to provide the highest performance. I am also interested in high-speed scientific processing, in particular in exploring issues related to the memory system, Instruction Level Parallelism, and the growing problem of excess power consumption.

PROFESSIONAL EXPERIENCE

- Full Professor in the Department of Computer Science at the Unversity of California, Davis, July 2002 to present.
- Associate Professor in the Department of Computer Science at the University of California, Davis, July 1995 to June 2002
- Assistant Professor in the Department of Computer Science at the University of California, Davis, September 1989 to June 1995

PROFESSIONAL ACTIVITIES

- Associate Editor, IEEE Transactions on Computers (2000-2004)
- Editor-in-Chief, Journal of Instruction Level Parallelism (1999-2002)
- Associate Editor, Journal of Instruction Level Parallelism
- Co-General Chair for 32nd Annual IEEE/ACM International Symposium on Microarchitecture
- Chair, IEEE Technical Committee on Microprogramming and Microarchitecture (1992-1998)
- Member, IEEE Technical Advisory Board Executive Committee (TC Elections)
- Program Chair for 27th Annual IEEE/ACM International Symposium on Microarchitecture
- Member, Program Committee for the 23rd, 24th, 27th, 28th, and 33rd Annual International Symposium on Computer Architecture

- Program Committee member for the 24th, 26th, 28th, 29th, 30th, 31st, 32nd, and 35th Annual IEEE/ACM International Symposium on Microarchitecture
- Steering Committee member for the 26th, 27th, 28th, 29th, 30th, 31st, 32nd, 33rd, 34th, and 35th Annual IEEE/ACM International Symposium on Microarchitecture
- Member, Program Committee for the 14th International Symposium on High-Performance Computer Architecture (HPCA)
- Member, NSF Funding Panels (2003, 2004, 2005, 2007)
- Secretary/Treasurer, SIGARCH (2003-2007)

CAMPUS SERVICE

- Member, Committee on Committees, 2008-2011
- Chair, College of Engineering Executive Committee 2000-2002, 2003-2005, 2010
- Co-Chair, Time to Degree Task Force 2004-2007
- Chair, Undergraduate Council 2004-2005
- Chair, Special Committee on Minimum Progress 2004-2005
- Davis Representative, Systemwide Coordinating Council on Graduate Affairs, 2007-2008
- Member, Graduate Council, Undergraduate Council, Academic Computing Council, Undergraduate Advising Council, Executive Council, Geidt Hall Building Committee, Athletic Administrative Advisory Committee, etc.

REFEREED PUBLICATIONS

[AhGF12] V. Ahuja, D. Ghosal and M. Farrens, "Minimizing the Data Transfer Time Using Multicore End-System Aware Flow Bifurcation", *12th IEEE/ACM International Symposium on Cluster, Cloud and Grid Computing (CCGrid)*, Ottowa, Canada (May 13-16, 2012), pp. (to appear).

[NiFA12] C. Nitta, M. Farrens and V. Akella, "DCAF - A Directly Connected Arbitration-Free Photonic Crossbar for Energy-Efficient High Performance Computing", *26th IEEE International Parallel and Distributed Processing Symposium*, Shanghai, China (May 21-25, 2012), pp. (to appear).

[NiFA11] C. Nitta, M. Farrens and V. Akella, "Resilient Microring Resonator Based Photonic Networks", *Proceedings of the 44th Annual IEEE/ACM International Symposium on Microarchitecture*, Porto Alegre, Brazil (Dec 3-7, 2011), pp. 95-104.

[NMFA11] C. Nitta, K. Macdonald, M. Farrens and V. Akella, "Inferring packet dependencies to improve trace based simulation of on-chip networks ", *Proceedings of the 5th Annual IEEE/ACM International Symposium on Networks on Chips*, Pittsburgh, PA (May 1-4, 2011), pp. 153-160.

[NiFA11] C. Nitta, M. Farrens and V. Akella, "Addressing System-Level Trimming Issues in On-Chip Nanophotonic Networks", *Proceedings of the 17th International IEEE Symposium on High Performance Computer Architecture*, San Antonio, TX (Feb 12-16, 2011), pp. 122-131 .

[MAFA10] P. V. Mejia, R. Amirtharajah, M. Farrens and V. Akella, "Performance Evaluation of a Multicore System with Optically Connected Memory Modules", *Fourth ACM/IEEE International Symposium on Networks-on-Chip* , Grenoble, France (May 3-6, 2010), pp. 215-222 .

[HBAA08] A. Hadke, T. Benavides, V. Akella, R. Amirtharajah and M. Farrens, “Design and Evaluation of an Optical CPU-DRAM Interconnect”, *Proceedings of the IEEE International Conference on Computer Design (ICCD): Green Computing*, Lake Tahoe, CA (October 12-15, 2008), pp. 492-497.

[NiFa08] C. Nitta and M. Farrens, “Techniques for Increasing Effective Data Bandwidth”, *Proceedings of the IEEE International Conference on Computer Design (ICCD): Green Computing*, Lake Tahoe, CA (October 12-15, 2008), pp. 492-497.

[CoFa08] P. Congdon and M. Farrens, “Packet Prediction for Speculative Cut-Through Switching”, *ACM/IEEE Symposium on Architectures for Networking and Communications Systems*, San Jose, CA (November 6-7, 2008), pp. 514-519.

[OsCF02] M. Oskin, F. Chong and M. Farrens, “Using Statistical and Symbolic Simulation for Microprocessor Evaluation”, *Journal of Instruction Level Parallelism,* vol. 4 (September 2002).

[LeT01] H. Lee, G. Tyson and M. Farrens, “Improving Bandwidth Utilization using Eager Writeback”, *Journal of Instruction Level Parallelism,* vol. 3 (October 2001).

[KCDF01] D. Keen, F. T. Chong, P. Devanbu, M. Farrens, J. Brown, J. Hollfelder and X. T. Zhuang, “Memory issues in hardware-supported software safety ”, *ISCA Workshop on Memory Performance Issues*, Goteburg, Sweden (June 28-July 4, 2001).

[LeT00] H. Lee, G. Tyson and M. Farrens, “Eager Writeback - a Technique for Improving Bandwidth Utilization”, *Proceedings of the 33rd Annual IEEE/ACM International Symposium on Microarchitecture*, Monterey, CA (December 10-13, 2000), pp. 11-21.

[OsCF00] M. Oskin, F. Chong and M. Farrens, “HLS: Combining Statistical and Symbolic Simulation to Guide Microprocessor Designs”, *Proceedings of the 27th Annual IEEE/ACM International Symposium on Computer Architecture*, Vancouver, BC (June 12-14, 2000), pp. 71-82.

[SaHF00] P. Sallee, M. Haungs and M. Farrens, “Branch Transition Rate: A New Metric for Improved Branch Classification Analysis”, *Proceedings of the 6th International IEEE Symposium on High Performance Computer Architecture*, Toulouse, France (January 10-12, 2000), pp. 241-250.

[RiFa00a] K. Rich and M. Farrens, “The Decoupled-Style Prefetch Architecture”, *Proceedings of the 6th International Euro-Par Conference*, Munich, Germany (August 28-September 1, 2000), pp. 989-993.

[RiFa00b] K. Rich and M. Farrens, “Code Partitioning in Decoupled Compilers”, *Proceedings of the 6th International Euro-Par Conference*, Munich, Germany (August 28-September 1, 2000), pp. 1008-1017.

[OHKC99] M. Oskin, J. Hensley, D. Keen, F. Chong, M. Farrens and A. Chopra, “Exploiting ILP in Page-based Intelligent Memory”, *Proceedings of the 32nd Annual IEEE/ACM International Symposium on Microarchitecture*, Haifa, Israel (November 16-18, 1999), pp. 208-218.

[RTTD98] J. Rivers, E. Tam, G. Tyson, E. Davidson and M. Farrens, “Utilizing Reuse Information in Data Cache Management”, *Proceedings of the 12th ACM International Conference on Supercomputing*, Melbourne, Australia (July 13-17th, 1998), pp. 449-456.

[TFMP97] G. Tyson, M. Farrens, J. Matthews and A. Pleszkun, “Managing Data Caches using Selective Cache Line Replacement”, *International Journal of Parallel Processing,* vol. 25, no. 3 (June 1997), pp. 213-242.

[TyFa96] G. Tyson and M. Farrens, “Evaluating the Effects of Predicated Execution on Branch Prediction”, *International Journal of Parallel Processing,* vol. 24, no. 2 (1996), pp. 159-186.

[TMFP95] G. Tyson, J. Matthews, M. Farrens and A. Pleszkun, “A Modified Approach to Data Cache Management”, *Proceedings of the 28th Annual International Symposium on Microarchitecture*, Ann Arbor, Michigan (November 29 - December 1, 1995), pp. 93-103.

[TyFa94] G. Tyson and M. Farrens, “Code Scheduling for Multiple Instruction Stream Architectures”, *International Journal of Parallel Processing,* vol. 22, no. 3 (1994), pp. 243-272.

[FaTP94] M. Farrens, G. Tyson and A. Pleszkun, “A Study of Single-Chip Processor/Cache Organizations for Large Numbers of Transistors”, *Proceedings of the 21st Annual Symposium on Computer Architecture*, Chicago, IL (April 18-21, 1994), pp. 338-347.

[HCLF94] D. G. Howitt, S. J. Chen, T. D. Ly, S. N. Farrens, M. K. Farrens, A. B. Harker and J. F. Flintoff, “Some Recent Advances in the Analysis of Materials in the SEM”, *VI Journadas De Microscopia Electronica*, Maracaibo (July 1994), pp. 70-81.

[HoLF93] D. G. Howitt, T. D. Ly and M. K. Farrens, “An Alternative Approach to Image Reconstruction in the SEM”, *Acta Microscopia,* vol. 2, no. 2 (November 1993), pp. 110-127.

[TyFa93] G. Tyson and M. Farrens, “Techniques for Extracting Instruction Level Parallelism on MIMD Architectures”, *Proceedings of the 26th Annual International Symposium on Microarchitecture*, Austin, Texas (December 1-3, 1993), pp. 128-137.

[FaNN93] M. Farrens, P. Nico and P. Ng, “A Comparison of Superscalar and Decoupled Access/Execute Architectures”, *Proceedings of the 26th Annual International Symposium on Microarchitecture*, Austin, Texas (December 1-3, 1993), pp. 100-103.

[TyFP92] G. Tyson, M. Farrens and A. Pleszkun, “MISC: A Multiple Instruction Stream Computer”, *Proceedings of the 25th Annual International Symposium on Microarchitecture*, Portland, Oregon (December 1-4, 1992), pp. 193-196.

[PaFT92] A. Park, M. Farrens and G. Tyson, “Modifying VM Hardware to Reduce Address Pin Requirements”, *Proceedings of the 25th Annual International Symposium on Microarchitecture*, Portland, Oregon (December 1-4, 1992), pp. 210-213.

[FPFN92] M. K. Farrens, A. Park, R. Fanfelle, P. Ng and G. Tyson, “A Partitioned Translation Lookaside Buffer Approach to Reducing Address Bandwidth”, *Proceedings of the 19th Annual Symposium on Computer Architecture*, Queensland, Australia (May 19-21, 1992), pp. 435.

[FaPW92] M. Farrens, A. Park and A. Woodruff, “CCHIME: A Cache Coherent Hybrid Interconnected Memory Extension”, *Sixth International Parallel Processing Symposium*, Hollywood, CA (March 1992), pp. 573-577.

[FaWW91] M. K. Farrens, B. R. Wetmore and A. G. Woodruff, “Alleviation of Tree Saturation in Multistage Interconnection Networks”, *Proceedings of Supercomputing ’91*, Albuquerque, New Mexico

(November 18-20, 1991), pp. 400-409.

[FaPa91] M. Farrens and A. Park, “Workload and Implementation Considerations for Dynamic Base Register Caching”, *Proceedings of the 24th Annual International Symposium on Microarchitecture*, Albuquerque, New Mexico (November 18-20, 1991), pp. 62-68.

[BePF91] J. Becker, A. Park and M. Farrens, “An Analysis of the Information Content of Address Reference Streams”, *Proceedings of the 24th Annual International Symposium on Microarchitecture*, Albuquerque, New Mexico (November 18-20, 1991), pp. 19-24.

[FaPl91] M. Farrens and A. Pleszkun, “Strategies for Achieving Improved Processor Throughput”, *Proceedings of the Eighteenth Annual International Symposium on Computer Architecture*, Toronto, Canada (May 27-30, 1991), pp. 362-369.

[FaPa91] M. Farrens and A. Park, “Dynamic Base Register Caching: A Technique for Reducing Address Bus Width”, *Proceedings of the Eighteenth Annual International Symposium on Computer Architecture*, Toronto, Canada (May 27-30, 1991), pp. 128-137.

[FaPl91] M. Farrens and A. Pleszkun, “Overview of the PIPE Processor Implementation”, *Proceedings of the 24th Annual Hawaii International Conference on System Sciences*, Kapaa, Kauai (January 9-11, 1991), pp. 433-443.

[FaPl89] M. K. Farrens and A. R. Pleszkun, “Improving the Performance of Small On-Chip Instruction Caches”, *Proceedings of the Sixteenth Annual International Symposium on Computer Architecture*, vol. 17, no. 3 (June 1989), pp. 234-241.

SELECTED AWARDS AND GRANTS

TITLE: Improving Trace Based Simulation of On-Chip Networks
AGENCY: NSF
AMOUNT: $448,835
PERIOD: 7/11-8/14

TITLE: Scaling the Performance of Network Security Applications Using Massively Parallel Processing Array (MPPA) Architectures
AGENCY: NSF
AMOUNT: $391,000
PERIOD: 9/10-8/13

TITLE: Estimating the End-system Network I/O Bottleneck Rate to Optimize Transport Layer Performance
AGENCY: NSF
AMOUNT: $410,946
PERIOD: 8/09-7/12

TITLE: Improving System Functionality using Monitoring Processors
AGENCY: NSF

AMOUNT: $370,508
PERIOD: 9/01-8/04

TITLE: Multi-Level Parallel Execution on Decoupled Systems
AGENCY: NSF
AMOUNT: $551,242
PERIOD: 8/98-7/01

TITLE: High Performance Single Chip VLSI Processors
AGENCY: NSF Young Investigator Awards
AMOUNT: $263,480
PERIOD: 6/92-5/97

TITLE: Reducing the Processor/Memory Bottleneck
AGENCY: NSF Research Experience for Undergraduates
AMOUNT: $10,000
PERIOD: 8/97-7/98

TITLE: Reducing I/O Pin Requirements for VLSI Processors
AGENCY: NSF
AMOUNT: $65,983
PERIOD: 12/93-11/95

TITLE: Techniques for Managing the Memory Hierarchy
AGENCY: SUN Microsystems
AMOUNT: $36,000
PERIOD: 12/95-11/96

TITLE: High Performance Single Chip VLSI Processors
AGENCY: NSF Research Experience for Undergraduates
AMOUNT: $10,000
PERIOD: 12/93-11/94

TITLE: Software Technology for Distributed Servers
AGENCY: SUN Microsystems Supercomputer Research Center
AMOUNT: $51,000
PERIOD: 1/93-12/93

TITLE: A Shared Functional Unit Approach to Improving Processor Throughput
AGENCY: UC MICRO
AMOUNT: $24,921
PERIOD: 7/91-6/92

TITLE: Evaluating the Effectiveness of Architectural I/O Queues
AGENCY: NSF Research Initiation Award
AMOUNT: $59,000
PERIOD: 6/90-5/92