1. (12) **True or False:**

(1) DRAM and Disk access times are rapidly converging.

(1) Measuring performance on multiprocessors using linear speedup instead of execution time is a bad idea.

(1) Computer systems achieve 99.999% availability ("five nines"), as advertised.

(1) Computer components fail suddenly, with little warning.

(1) Amdahl's law applies to parallel computers.

(1) You can predict cache performance of Program A by analyzing Program B.

(1) Linear speedups are needed to make multiprocessors cost-effective.

(1) Scalability is almost free.

(1) A program's locality behavior is constant over the run of an entire program.

(1) Operating systems are the best place to schedule disk accesses.

(1) Communication is not a significant problem for parallel processor systems.

(1) The instruction set architecture does not impact the implementability of a virtual machine monitor.

2. (3) What is the goal of the memory heirarchy? What two principles make it work?

3. (15) What do the following acronyms stand for:

| | | |
|---|---|---|
| SMT | SMP | MTTF |
| COMA | RAID | RAW |
| NUMA | MPP | DSM |
| MTTR | SRAM | ILP |
| VMM | OLTP | TPC |

4. (1) Which benchmarks are most affected by the window size? (Circle the correct answer)

integer float equally affected

5. (1) Which benchmarks are most affected by the accuracy of the branch predictor? (Circle the correct answer)

integer float equally affected

6. (1) Alias analysis has the most impact on which benchmark? (Circle the correct answer)

integer float equally affected

7. (7) Which of the following does the book list as advanced optimizations of cache performance? (Circle the correct answer)

| | |
|---|---|
| Small and simple caches | Larger block size |
| Bigger caches | Way prediction |
| Trace caches | Higher associativity |
| Multilevel caches | Pipelined caches |
| Non-blocking caches | Multibanked caches |
| Compiler optimizations | Victim cache |

**Short Answers:**

8. (3) What is a victim cache, and how does it work?

9. (4) Cache misses can be catagorized into 4 different types. What are the four types of cache misses?

10. (6) What is an instruction window? How does it impact ILP?

11. (7) What is simultaneous multithreading? What characteristics of multi-issue processors is this trying to take advantage of? (Be relatively detailed in your answer)

12. (8) What is Cache Coherence, and why is it necessary? Snooping is one main approach to providing coherence - state what the other main approach is, and briefly outline how each of them work.

13. (8) What type of operation is required to support synchronization? (Hint - the answer I'm looking for starts with an "A"). What pair of instructions are used to implement a lock in RISC systems (as described in the text)? Describe how this pair works together in order to accomplish the goal.

14. (8) Assume a relatively large fully associative write-back cache that contains no valid data. Given the following sequence of 5 memory operations (the address of the operation is in the square brackets):

WriteMem[100]
WriteMem[100]
ReadMem[200]
WriteMem[200]
WriteMem[100]

What are the number of hits and misses when using write allocate versus no-write allocate?

15. (8) Suppose you want to achieve a speedup of 80 with 100 processors. What fraction of the original computation can be sequential? (Full credit if you show your work, half-credit if you just write the answer.)

16. (8) Assume that words A and B are in two different locations in the same cache block, which is in the shared state in the caches of both P1 and P2. In the following sequence of events, identify each miss as either a true sharing miss, a false miss, a sharing miss, or a hit. (Any miss that would occur if the block size were one word is referred to as a true sharing miss.)

| Time | P1 | P2 |
|---|---|---|
| 1 | Write A | |
| 2 | | Read B |
| 3 | Write A | |
| 4 | | Write B |
| 5 | Read B | |

For example, the event at time 1 is a true sharing miss, because A was read by P2 and needs to be invalidated from P2. For each event 2-5, list what type of miss occurs.