(1) [3] When we talk about the number of operands in an instruction (a 1-operand or a 2-operand, for example), what do we mean?

(2) [5] Clock rates have grown by a factor of 1000 while power consumed has only grown by a factor of 30. How was this accomplished? Why was this so effective? Why is this technique no longer effective?

(3) [4] As minimum feature sizes decrease, a) what happens to power density? b) what happens to wire resistance, and why?

(4) [4] It is difficult for the internal processing elements on a chip to communicate with the outside world (things that are on other chips, for example). Explain why that is.

(5) [4] What is "Yield"? Is it important? Why or why not?

(6) [6] There are two different types of power consumption, static and dynamic. Which one contributed the most to overall power consumption 20 years ago? What is the situation now, and why has it changed?

(7) [4] What is a benchmark program? What is the **perfect** benchmark?

(8) [4] Benchmarks need to change over time. Why?

(9) [4] Machines today use registers - often as many as they can. Give 2 advantages and 2 disadvantages to using registers.

(10) [4] Register allocation is a very effective and useful compiler optimization. However, it cannot be used in certain situations for correctness reasons - explain why.

(11) [4] What are the 3 types of data hazards? Which one can be solved by using forwarding?

(12) [3] What is a "balanced" pipeline?

(13) [4] What are the 3 pipeline hazards? Which one can be solved by providing more resources?

(14) [2] What are the two primary goals of a compiler (in order)?

(15) [8] In an MOS device, there is a gate, drain, and source. Briefly explain how this device works. Drawing a picture is recommended.

(16) [6] What are the two main ways to define performance? How do they differ? Give an example task for each.

(17) [3] When dealing with control hazards, it is not enough to predict the branch direction - what else must we know?

(18) [4] In the 5-stage pipeline described in class, is it possible to have a WAR hazard? Why or why not?

(19) [5] Processor A requires 600 instructions to execute a given program, uses 1 cycles per instruction, and has a cycle time of 5 ns. Processor B requires 4 cycle per instruction, but only requires 120 instructions to do the same program. What must the cycle time of Processor B be in order to give the same CPU time as Processor A? (Show your work)

(20) [6] You are responsible for designing a new embedded processor, and for a variety of reasons you must use a fixed 14 bit instruction size. You would like to support 32 different operations, use a 3-operand instruction format, and have 16 registers. If it is possible to do this, draw what an instruction would look like. If it is not possible, explain why, and show what you would do to fix the problem.

(21) [5] An important program spends 60% of its time doing Integer operations, and 40% of its time doing floating point arithmetic. By redesigning the hardware you can either make the Floating Point unit 70% faster (take 30% as long), or the integer unit 50% faster (take 50% as long). Which should you do, and why?

(22) [8] The standard MIPS has a 5-stage pipeline, and uses a load delay slot. If the machine is redesigned to be an 8-stage pipeline, with the following stages:

F D RR E1 E2 M1 M2 WB (where RR stands for Register Read)

Assuming the machine has bypass/forwarding logic, how many load delay slots will this new design require if the memory returns the value at the end of M2? At the end of M1?

How many branch delay slots will this new design require, assuming the branch condition is calculated and available at the end of E1?

How many branch delay slots if the branch condition is calculated and available at the end of E2?