

Very Short Answer:

- (1) (4) What are the 4 different types of control flow changes?

- (2) (1) Do benchmarks remain valid indefinitely?

- (3) (1) If I am more interested in code size than performance, I will choose which kind of instruction encoding?

- (4) (2) Issuing multiple instructions per cycle puts tremendous pressure on what unit?

- (5) (1) Ignoring instruction set issues, what makes pipelining hard to implement?

- (6) (2) What is a "poison" bit?

- (7) (1) Out of Order completion makes supporting what very difficult?

- (8) (1) Are wire delays or transistors more likely to be the most significant limit on clock frequency in the future?

- (9) (2) Standard decoupled architectures split a program into two streams. What are they?

Short Answers:

- (10) (3) Most silicon dies are fairly small. Why are they not bigger?
- (11) (3) What is branch folding?
- (12) (3) Write down the 3-term CPU performance equation developed in class.
- (13) (6) There are 3 kinds of Hazards. List and give brief descriptions of all three.
- (14) (6) Predicated instructions cannot eliminate a branch instruction when that branch is part of what kind of program structure?

(15) (14) You are given the following code sequence:

```
LF   F6,34(R2)
LF   F2, 45(R3)
MULTF F0,F2,F4
SUBF  F7,F6,F2
DIVF  F1,F0,F6
ADDF  F6,F7,F2
```

Assume there are 8 logical and 16 physical registers. On the left below is the register mapping upon entering the code sequence. Your job is to fill in the mappings after the execution of the ADDF instruction, including the free list. of

BEFORE	
Logical	Physical
0	12
1	13
2	15
3	14
4	9
5	7
6	6
7	8

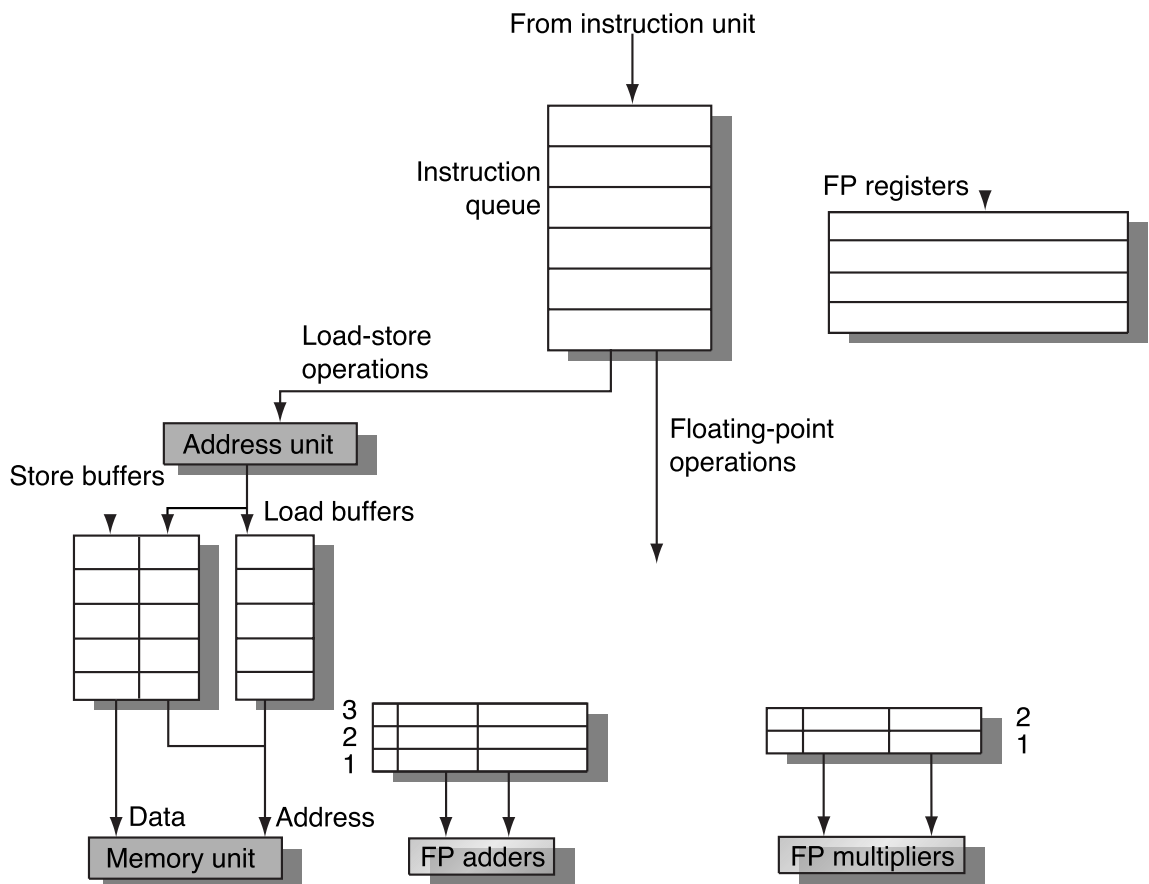
Free Pool: 0,1,2,3,4,5,10,11

AFTER	
Logical	Physical
0	
1	
2	
3	
4	
5	
6	
7	

Free Pool:

Now, rewrite the code sequence below using the actual physical register names instead of the logical ones.

- (16) (8) Below is a picture of some of the basic components of Tomasulo's algorithm. However, there are things missing. Draw in what is necessary to complete the picture.



(17) (7) Compare and contrast Superscalar with VLIW. Describe each, and list the advantages and disadvantages of each approach.

(18) (15) On the following page is the table used to describe scoreboarding. The contents of the table represent the state of the scoreboard at time 4. Your job is to fill in the table at time 8. Assume at time 8 the 2nd LF completes

- (19) (10) Assume that a processor with a single port to memory has a clock rate that is 1.10 times higher than the clock rate of the processor with dual ported memory. Data references constitute 30% of an instruction mix, and the ideal CPI of a pipelined processor without any structural hazards is 1. Disregarding any other performance losses, is the pipeline with or without the structural hazard faster, and by how much?

(20) (10) Suppose we have made the following measurements:

Frequency of floating point operations (other than square root) = 30%

Average CPI of floating point operations = 5.0

Average CPI of other instructions = 1.5

Frequency of square root = 3%

CPI of square root = 30

You have a choice - decrease the CPI of the square root by an order of magnitude, or decrease the average CPI of all floating point operations to 2.5. Which one of these should you do? (Show how you came to this conclusion, obviously! :-)