(1) (6) List at least 5 different addressing modes. Which addressing modes are used in Load/Store machines? Why?

(2) (5) The book lists many Compiler Optimizations. List 5 of them.

(3) (10) What are Benchmarks, and why are they important? List the 4 classes of benchmarks, give an example for each class, and tell me what the perfect benchmark would be.

(4) (10) Why is branch prediction important? What performance enhancing techniques have made it so? List 3 examples of existing Branch Prediction strategies in order of their (average) effectiveness.

(5) (8) There are 3 kinds of Hazards, Structural and two others. List the other two, give brief descriptions of all three, and some ways to alleviate the impact of each on processor performance.

(6) (6) There are 3 kinds of dependencies. List the 3, and give brief examples and descriptions of each.

(7) (10) Assume we have a machine where the CPI is 2.0 when all memory accesses hit in the cache. The only data accesses are loads and stores, and these total 40% of the instructions. If the miss penalty is 25 clock cycles and the miss rate is 2%, how much faster would the machine be if all instructions were cache hits?

(8) (20) Consider adding a new index addressing mode to DLX. The addressing mode adds two registers and an 11-bit signed offset to get the effective address.
Our compiler will be changed so that code sequences of the form

```
ADD   R1,R1,R2
LW    Rd,0(R1)       (or store)
```

will be replaced with a load (or store) using the new addressing mode. Use the overall average instruction frequencies given below in evaluating the addition.

Instruction	**compress**	**eqntott**	**espresso**	**gcc(cc1)**	**li**	**Integer Average**
load	19.8%	30.6%	20.9%	22.8%	31.3%	26%
store	5.6%	0.6%	5.1%	14.3%	16.7%	9%

a) Assume that the addressing mode can be used for 10% of the displacement loads and stores (accounting for both the frequency of this type of address calculation and the shorter offset). What is the ratio of instruction count on the enhanced DLX compared to the original DLX?

b) If the new addressing mode lengthens the clock cycle by 5%, which machine will be faster and by how much?

(9) (25) A shortcoming of the scoreboard approach occurs when multiple functional units that share input buses are waiting for a single result. The units cannot start simultaneously, but must serialize. This is not true of Tomasulo's algorithm. Give a code sequence that uses no more than 10 instructions and shows this problem. Assume the hardware configuration from figure 4.3 for the scoreboard, and figure 4.8 for Tomasulo's scheme. Use the FP latencies from figure 4.2. Indicate where the Tomasulo approach can continue, but the scoreboard approach must stall.