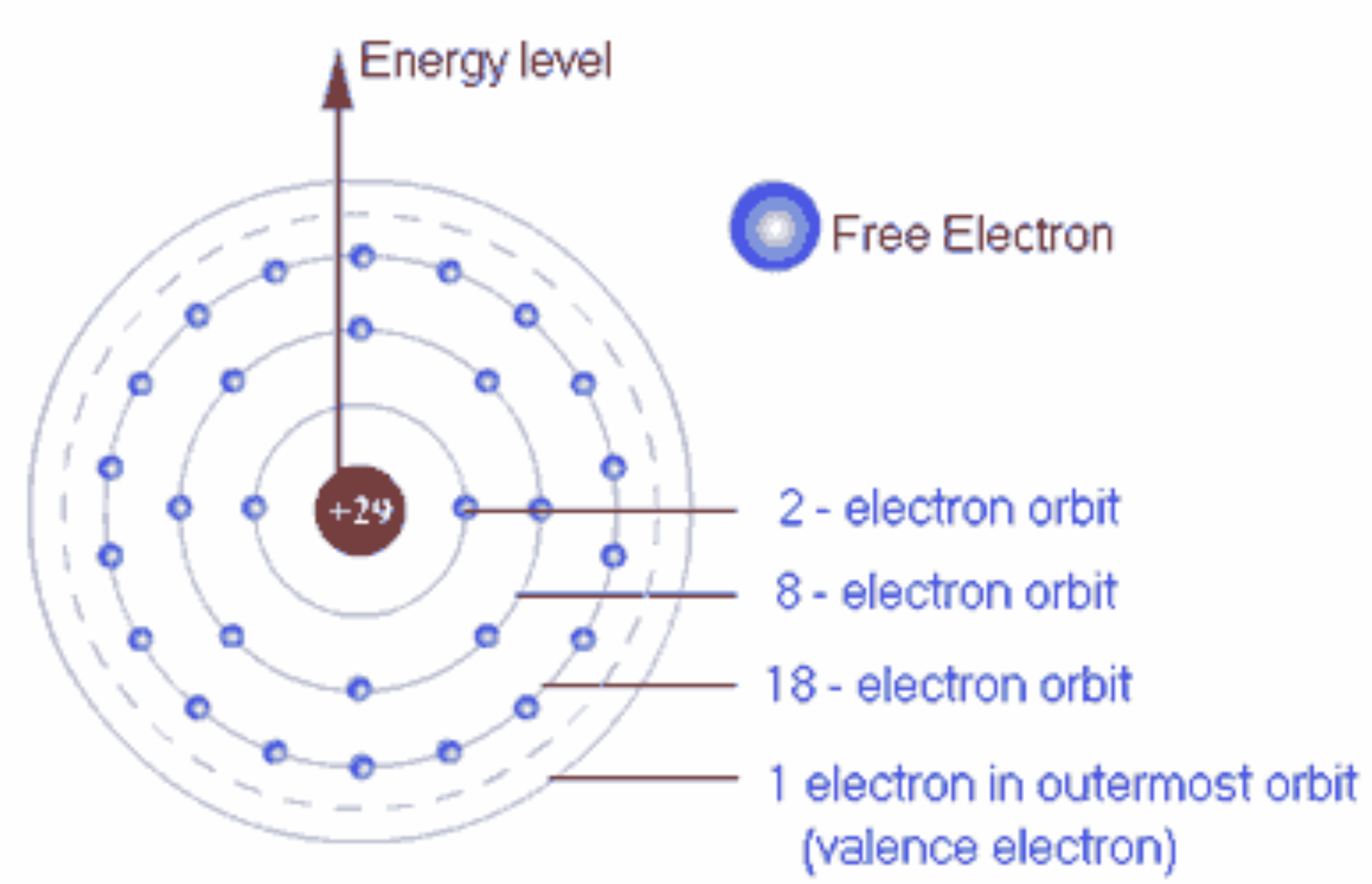
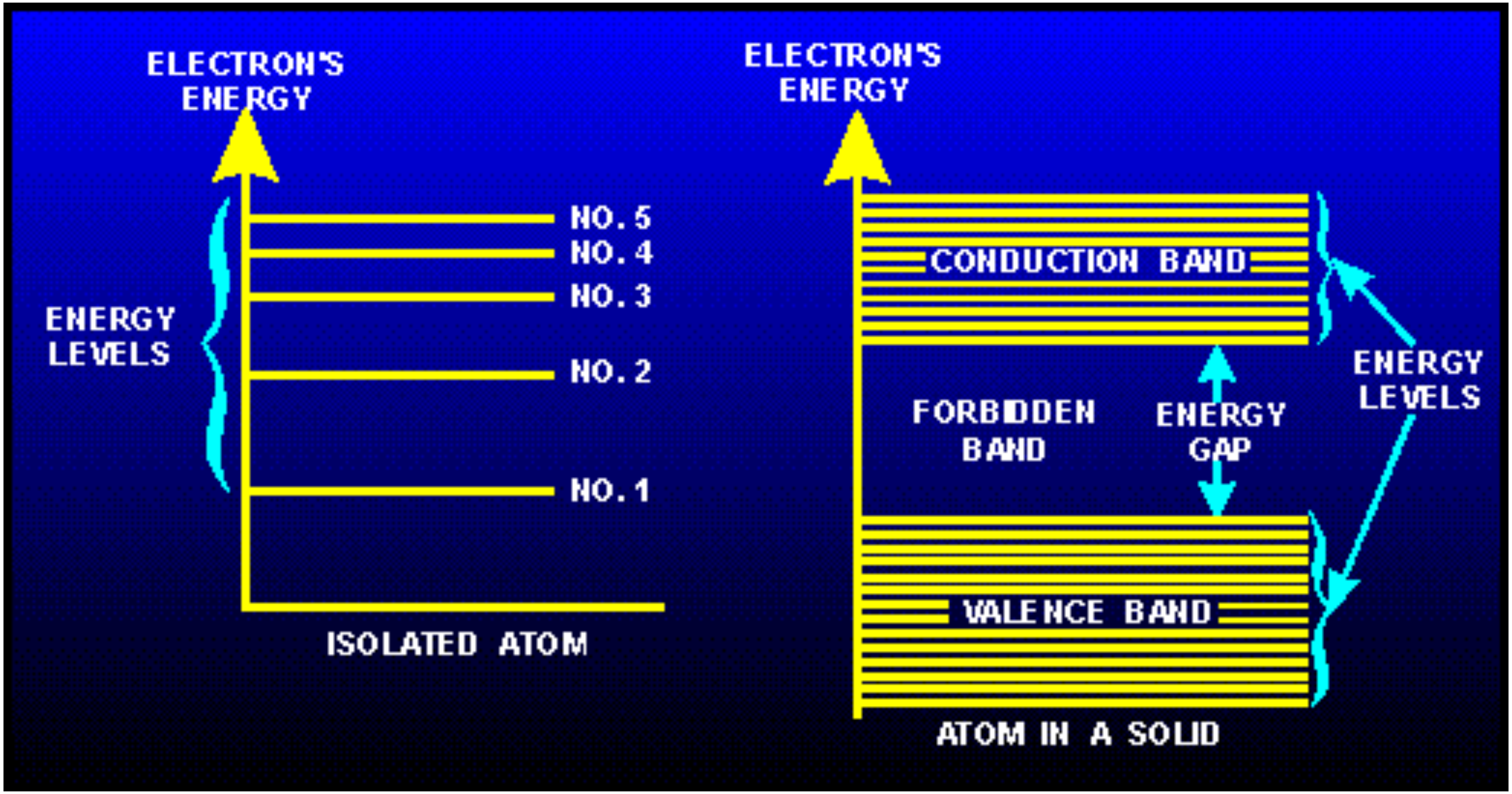
Technology Overview

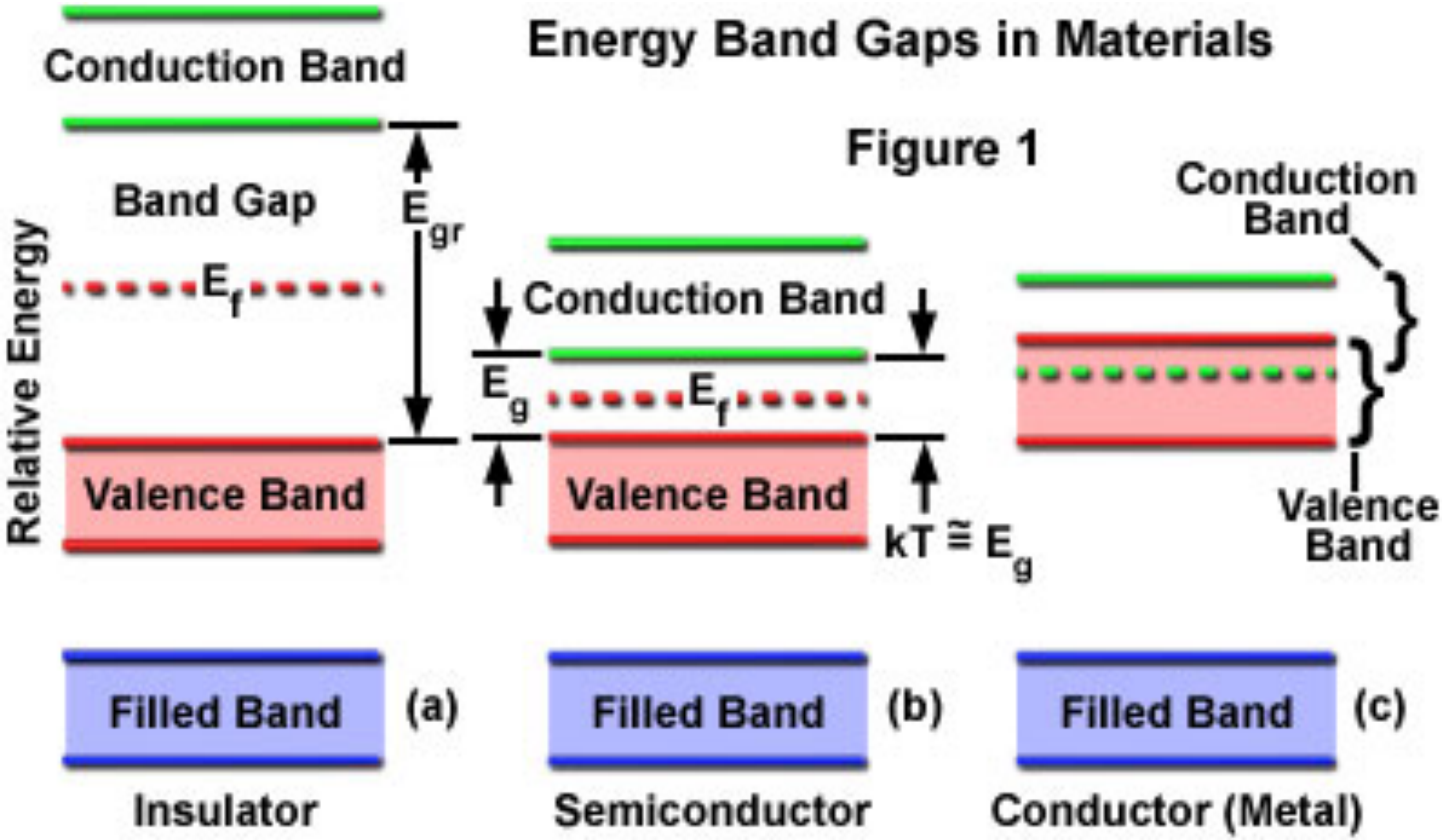
Atoms and Valence Electrons



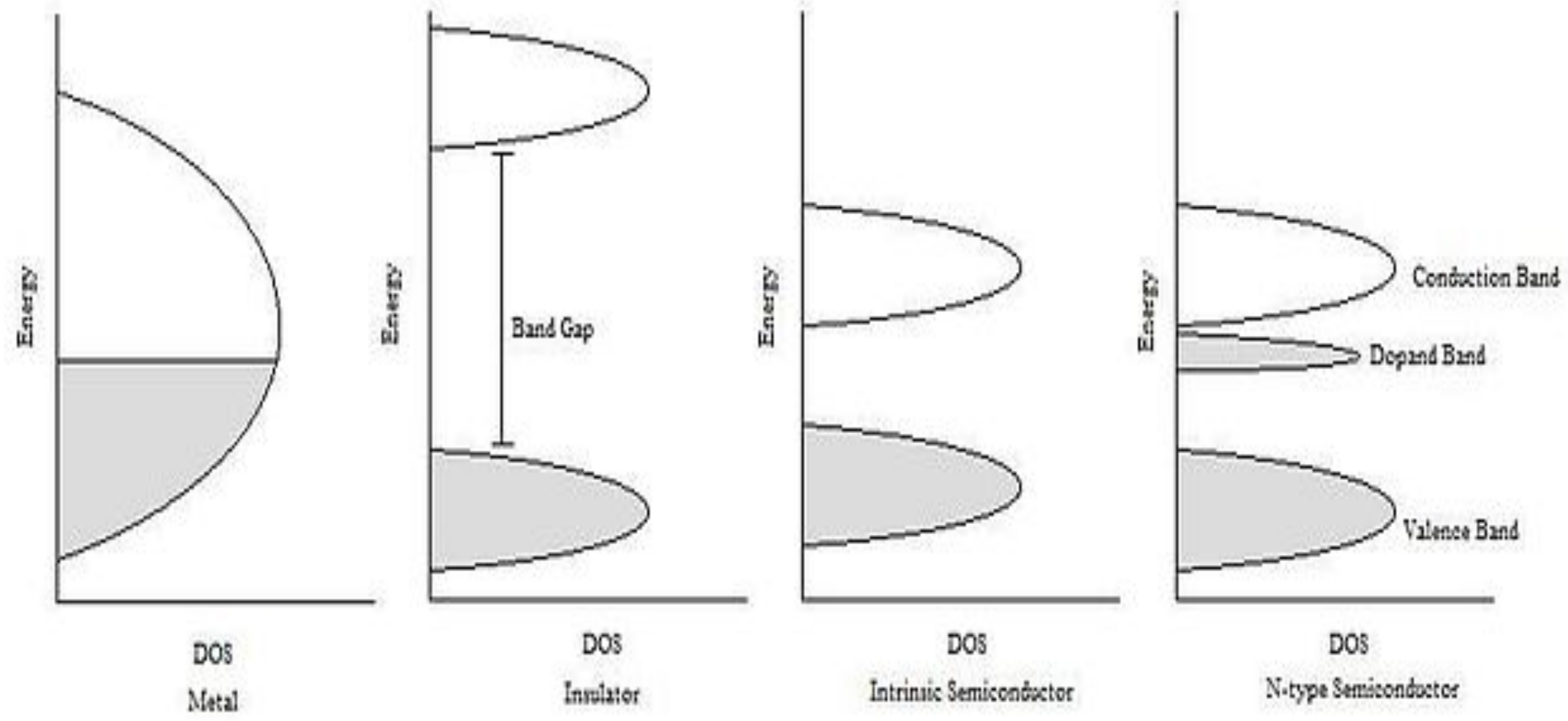
Conduction and Valence Bands



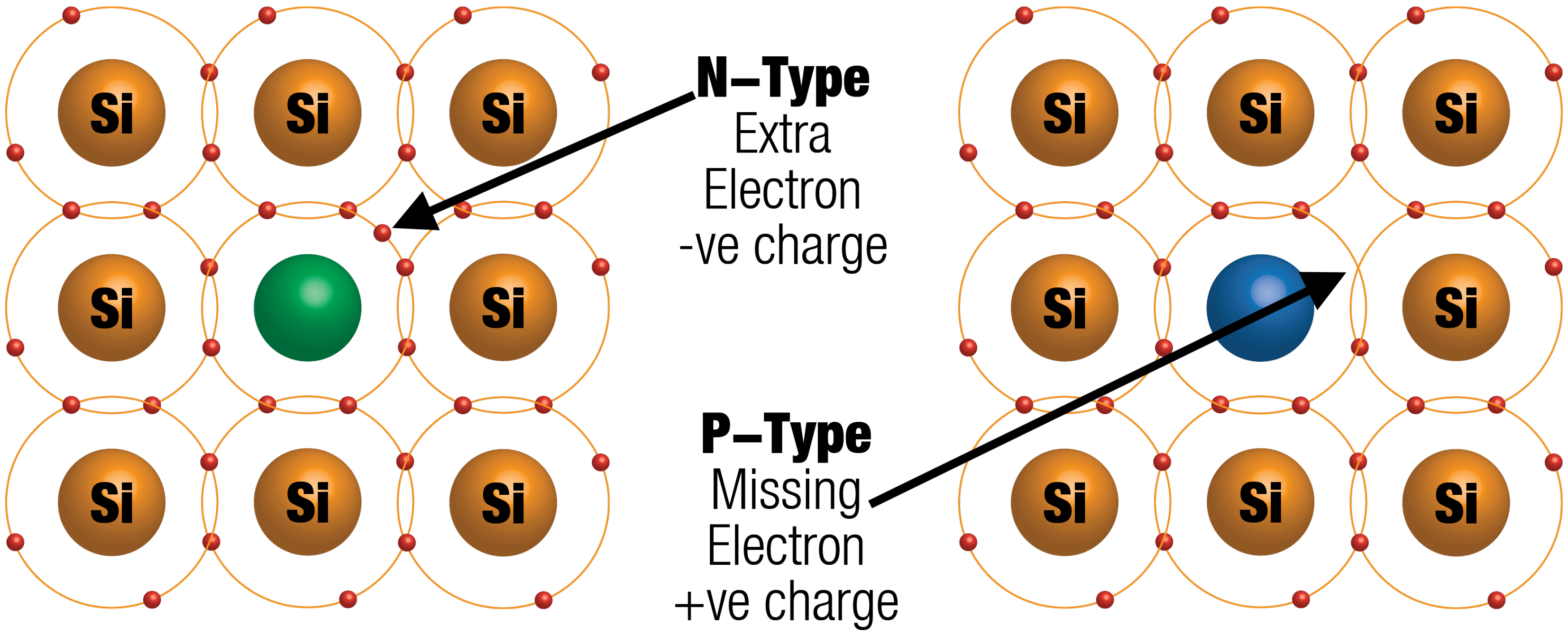
Energy Band Gaps in Materials



Band gap


Energy
DOS
Metal
Energy
Band Gap
DOS
Insulator
Energy
DOS
Intrinsic Semiconductor
Energy
Conduction Band
Dopand Band
Valence Band
DOS
N-type Semiconductor

N-type and P-type Doping



N–Type
Extra
Electron
-ve charge

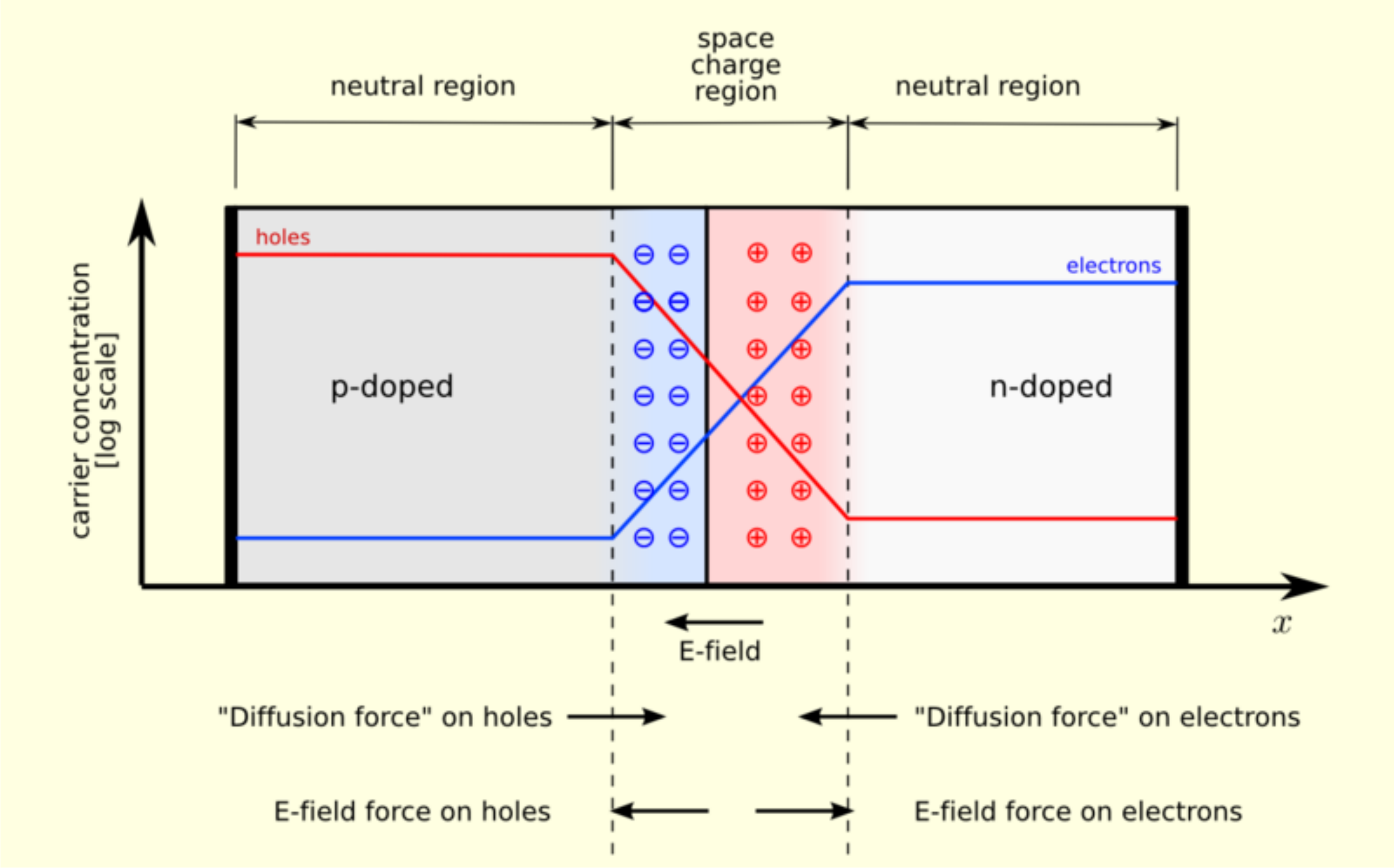
P–Type
Missing
Electron
+ve charge

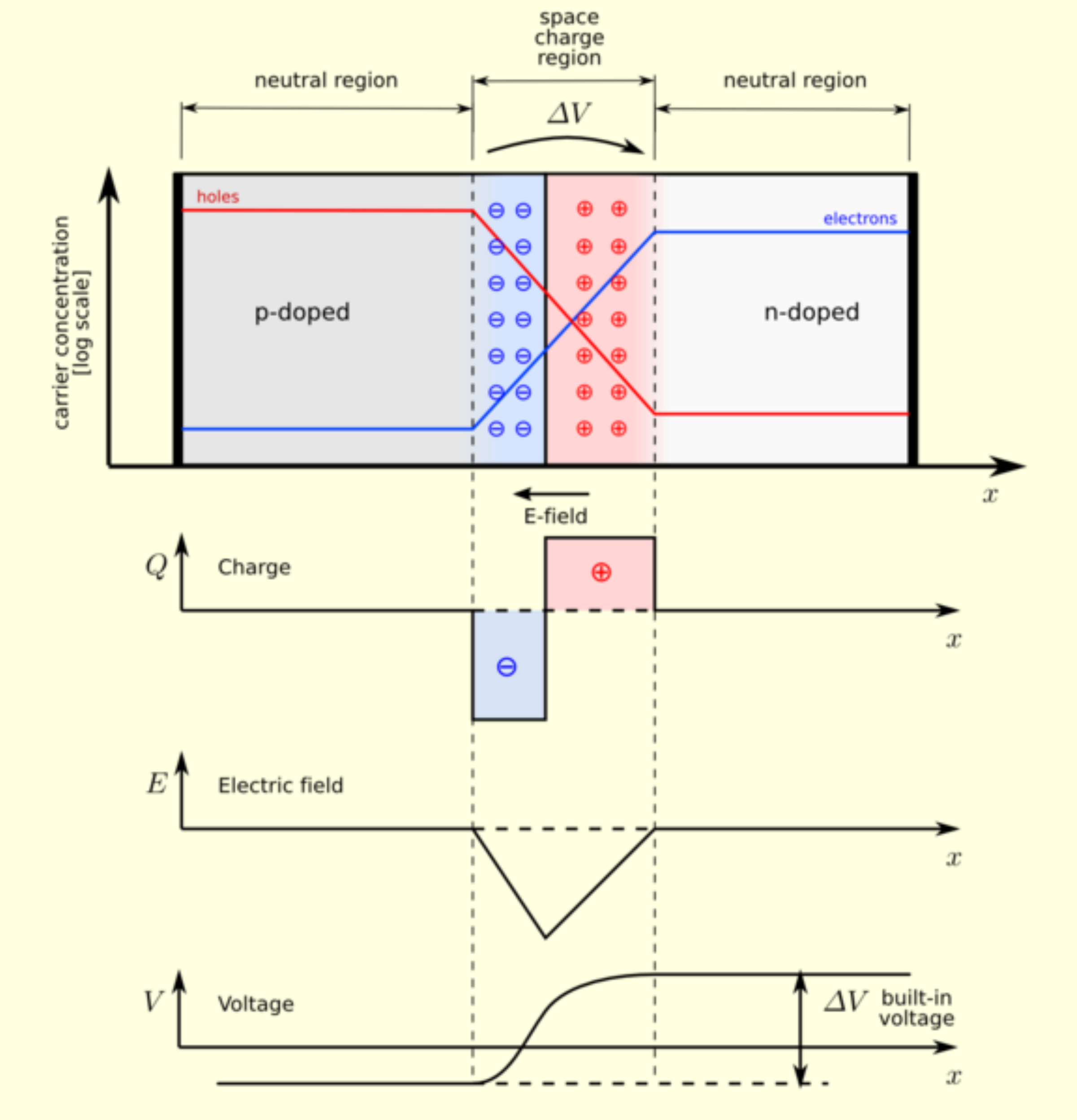
Silicon and Adjacent Atoms

5 B Boron 2.34	6 C Carbon 2.62	7 N Nitrogen 1.251
13 Al Aluminum 2.70	14 Si Silicon 2.33	15 P Phosphorus 1.82
31 Ga Gallium 5.91	32 Ge Germanium 5.32	33 As Arsenic 5.72

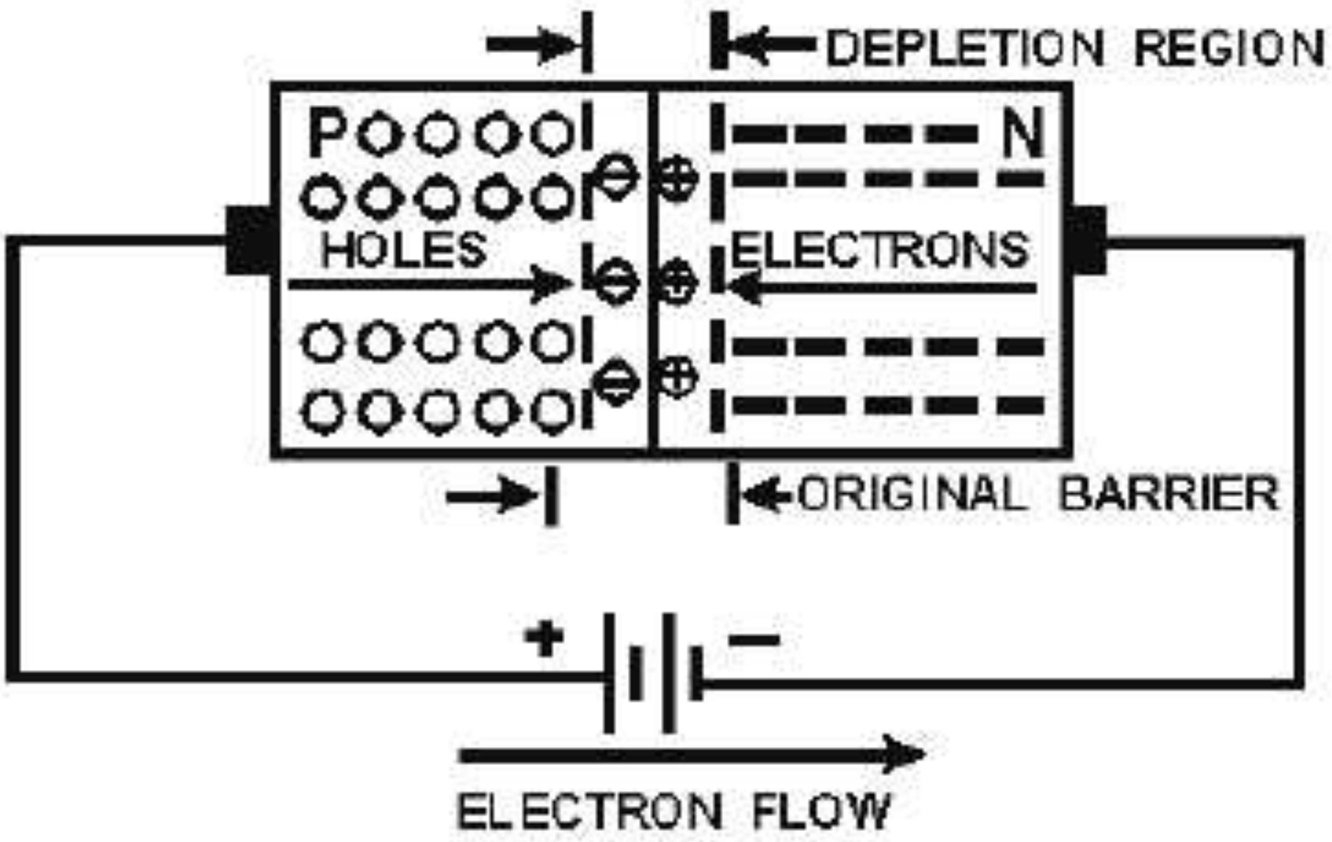
©2001 HowStuffWorks

PN Junction

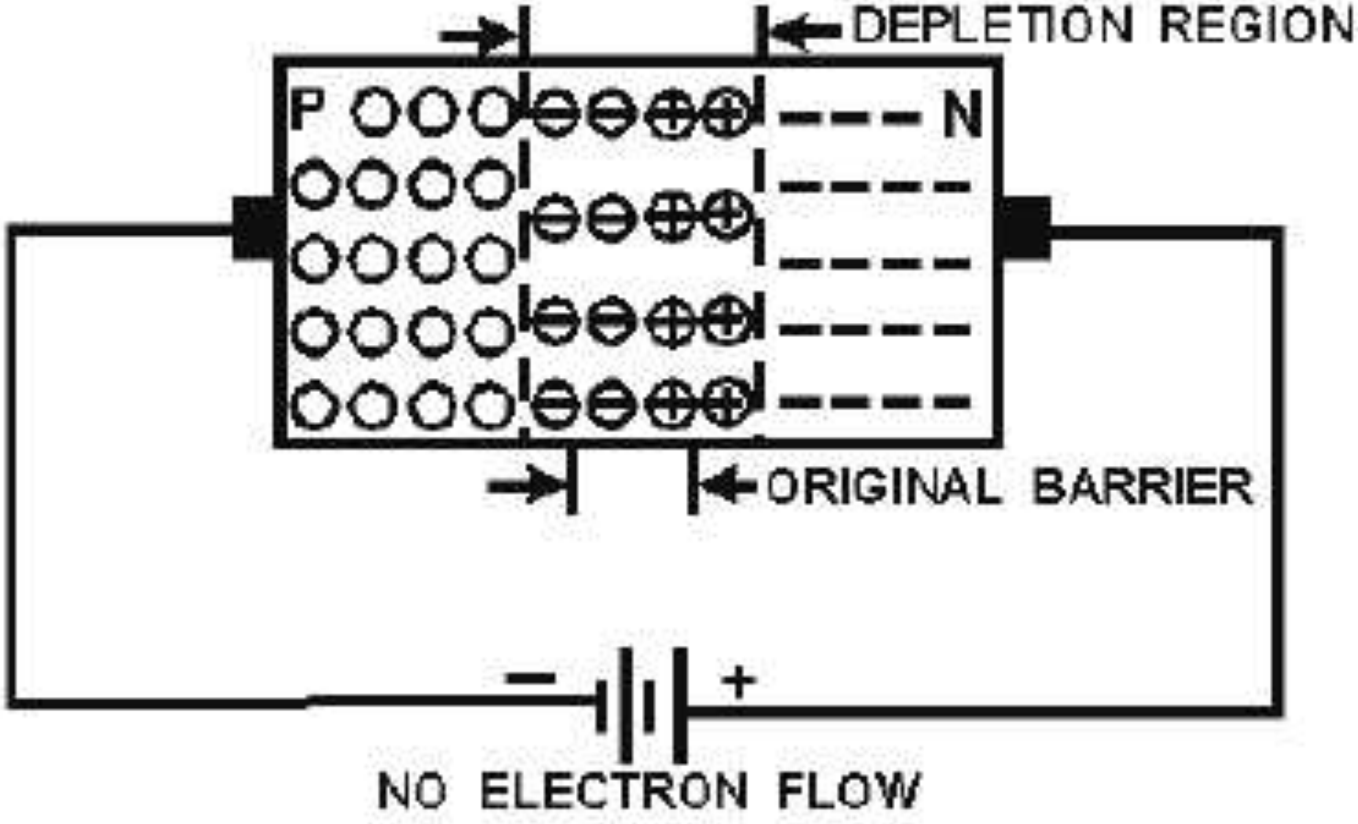

space
charge
region
neutral region
neutral region
holes
electrons
p-doped
n-doped
carrier concentration
[log scale]
x
E-field
"Diffusion force" on holes
"Diffusion force" on electrons
E-field force on holes
E-field force on electrons


space charge region
neutral region
neutral region
ΔV
holes
electrons
carrier concentration [log scale]
p-doped
n-doped
x
E-field
Q
Charge
x
E
Electric field
x
V
Voltage
ΔV
built-in voltage
x

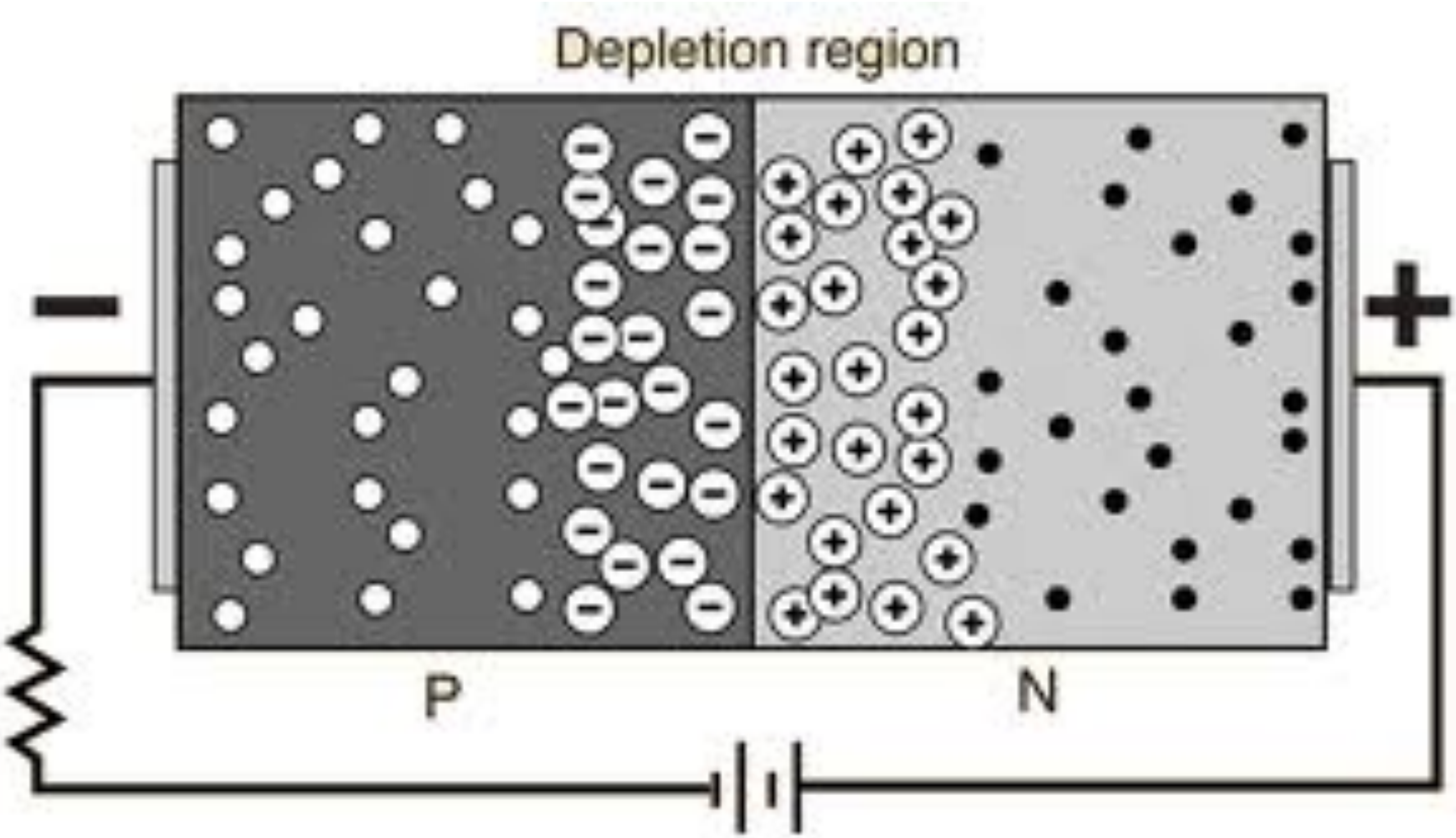
Forward Biased PN Junction



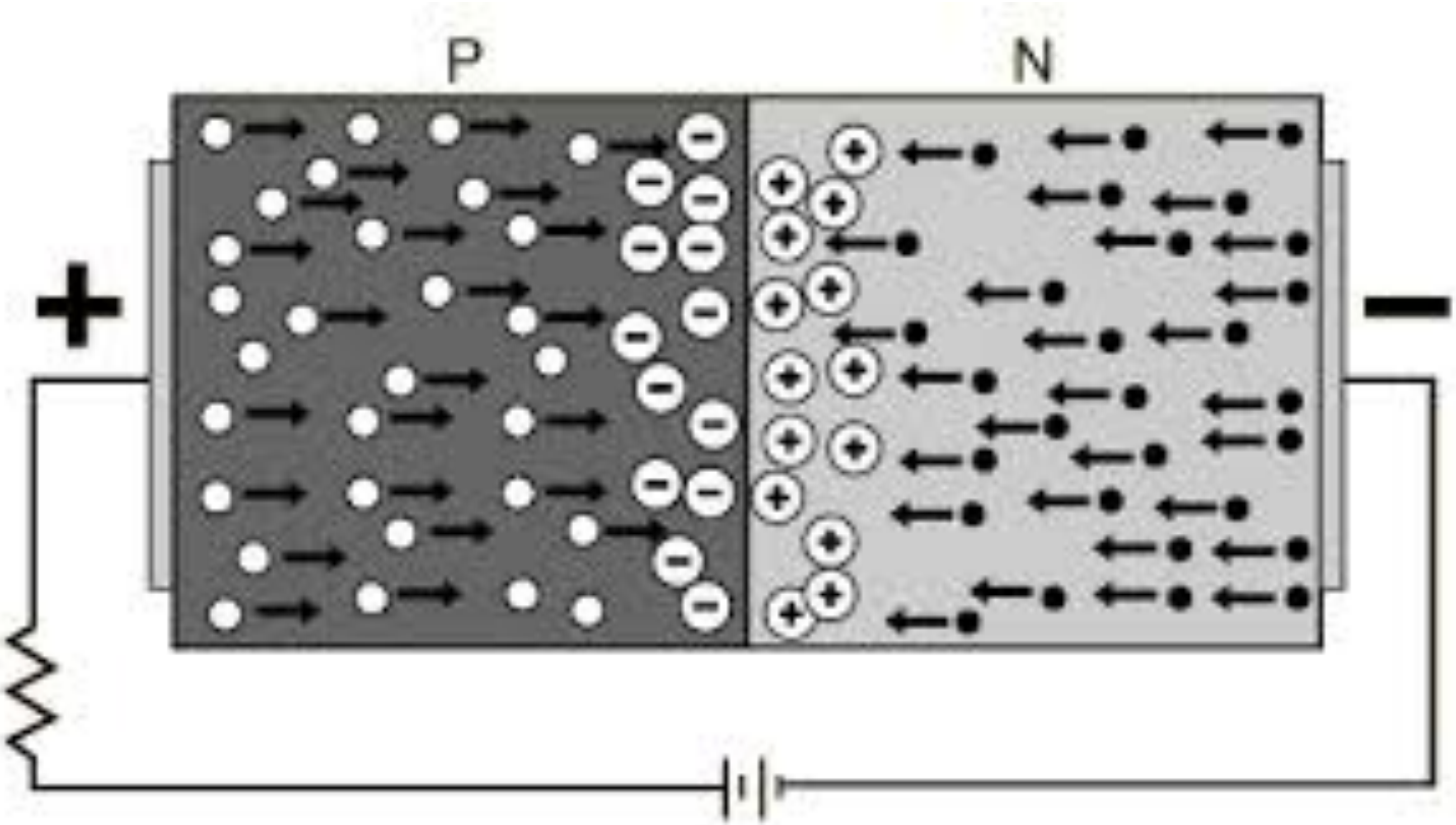
Reverse Biased PN Junction



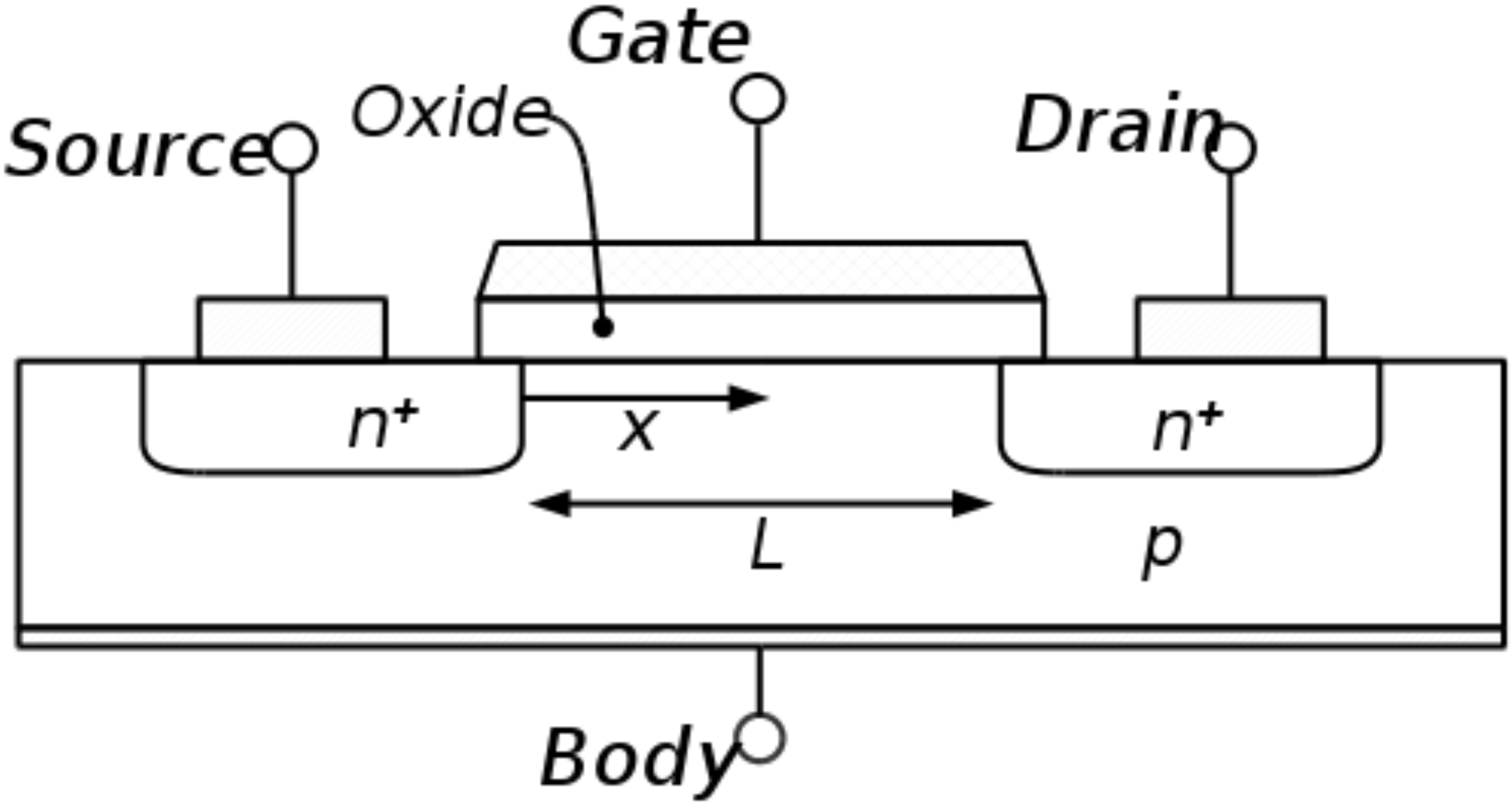
Reverse Biased PN Junction



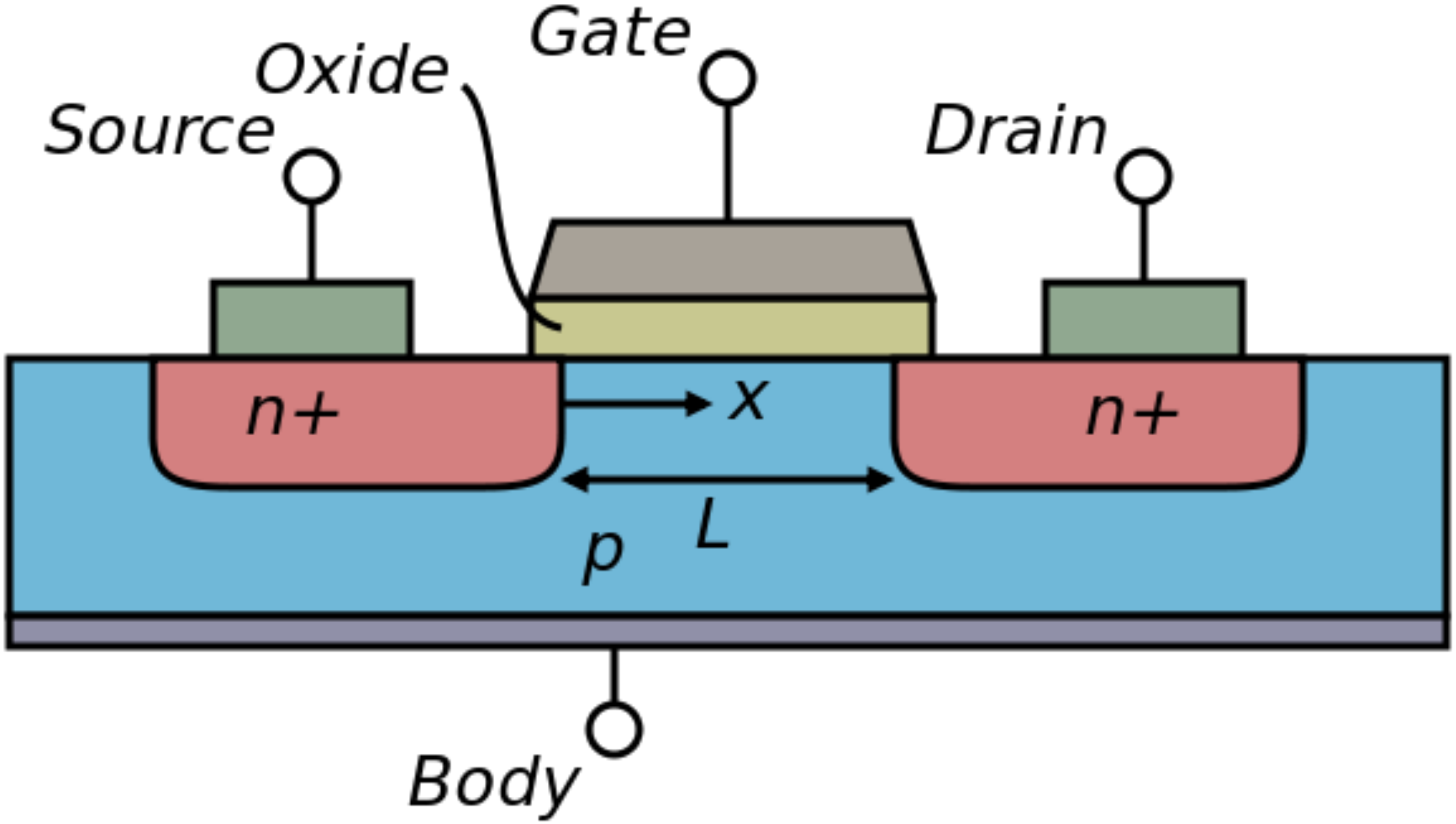
Forward Biased PN Junction



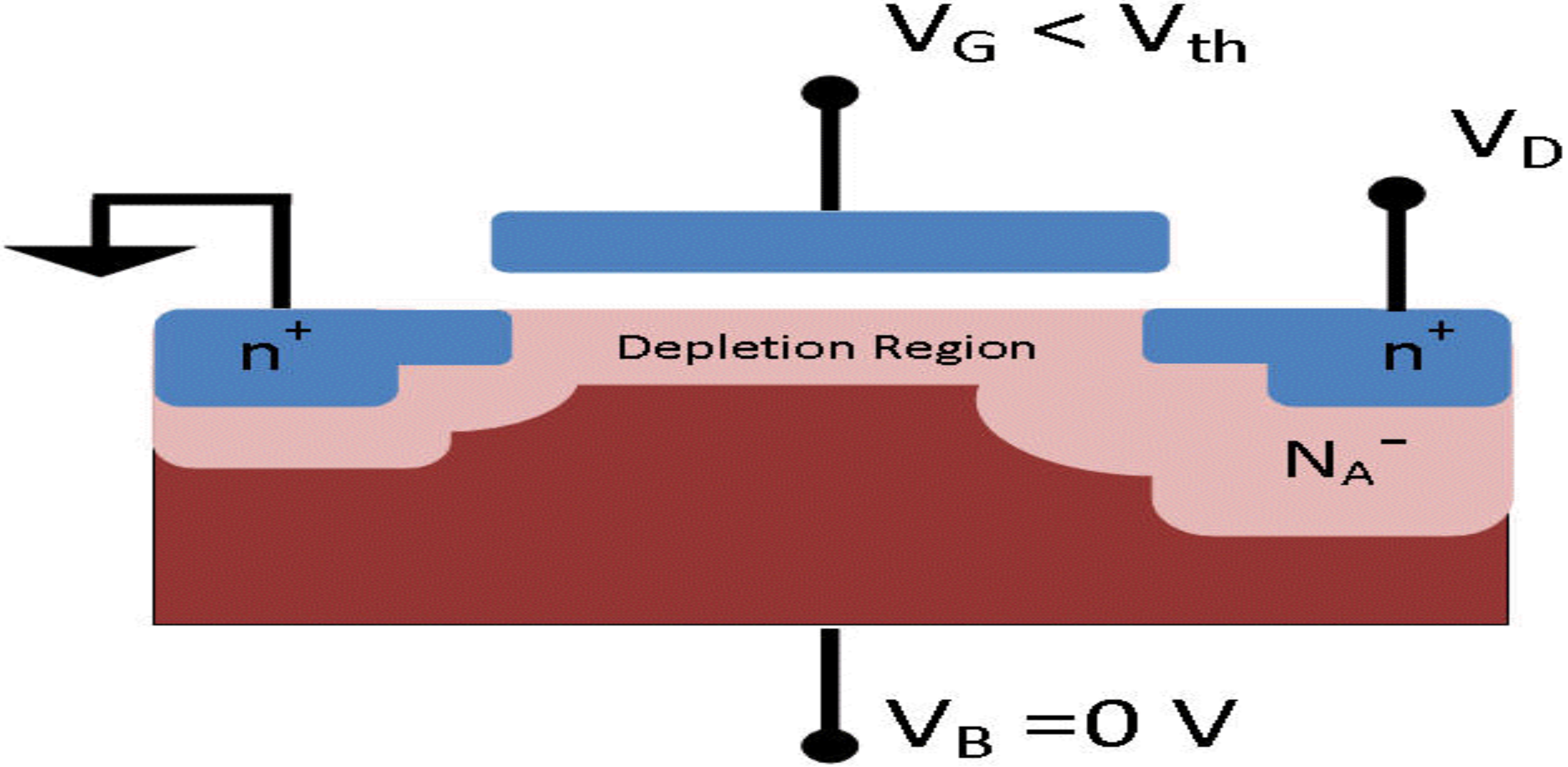
N-type MOSFET



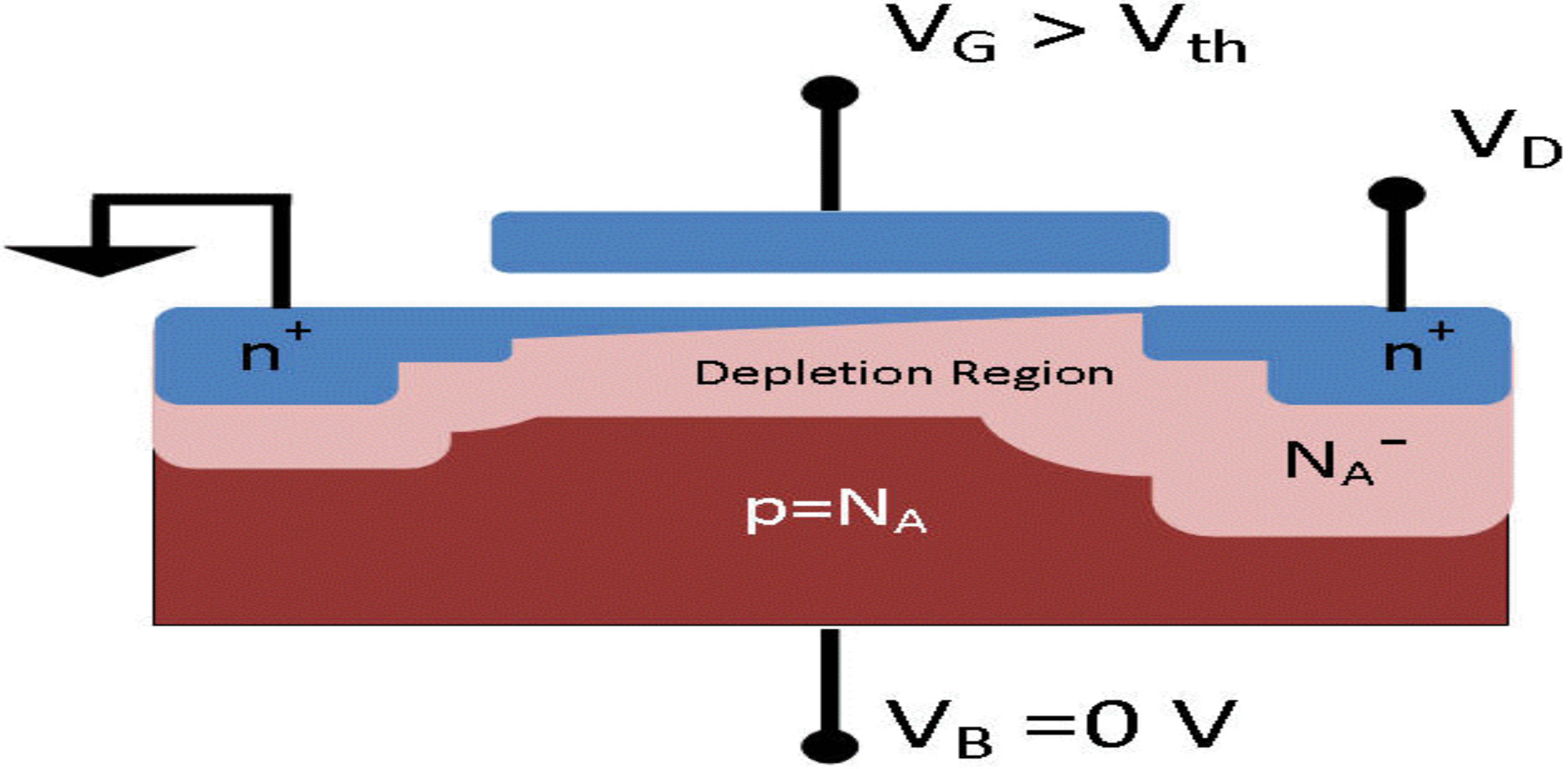
N-type MOSFET



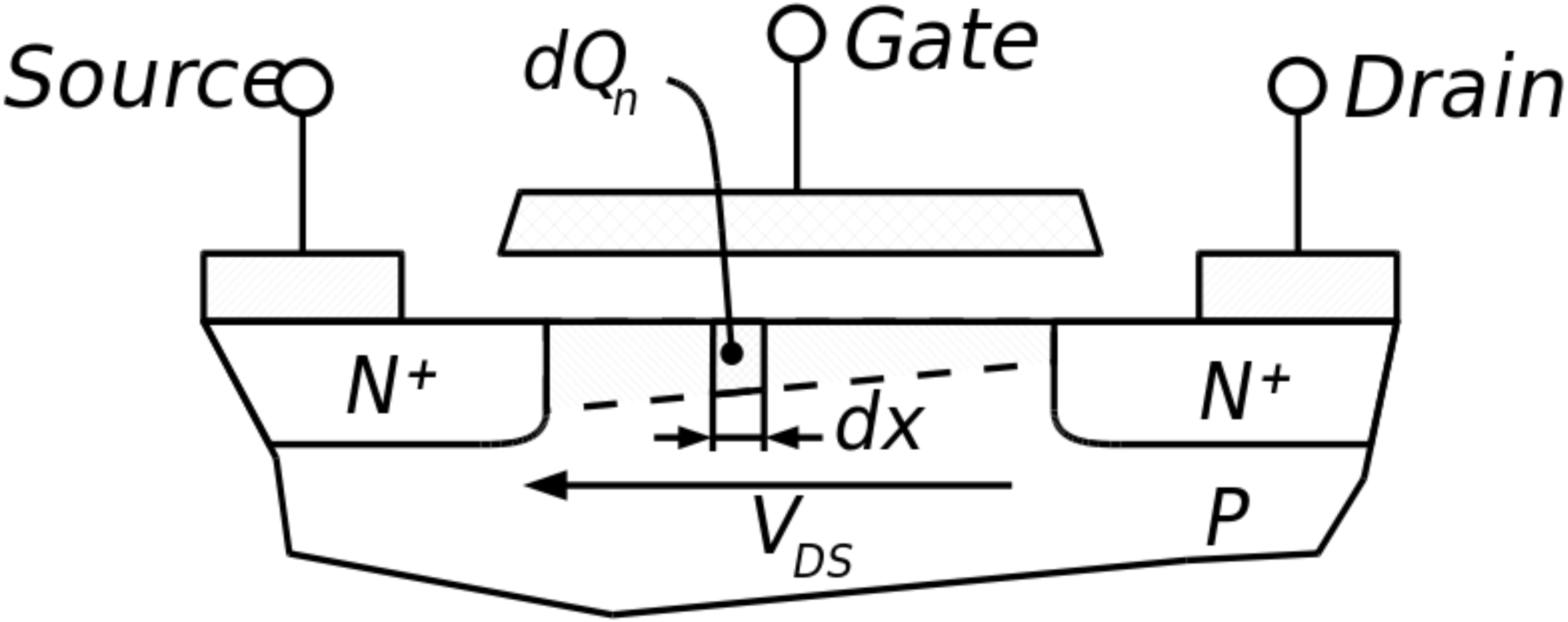
N-type MOSFET (off)



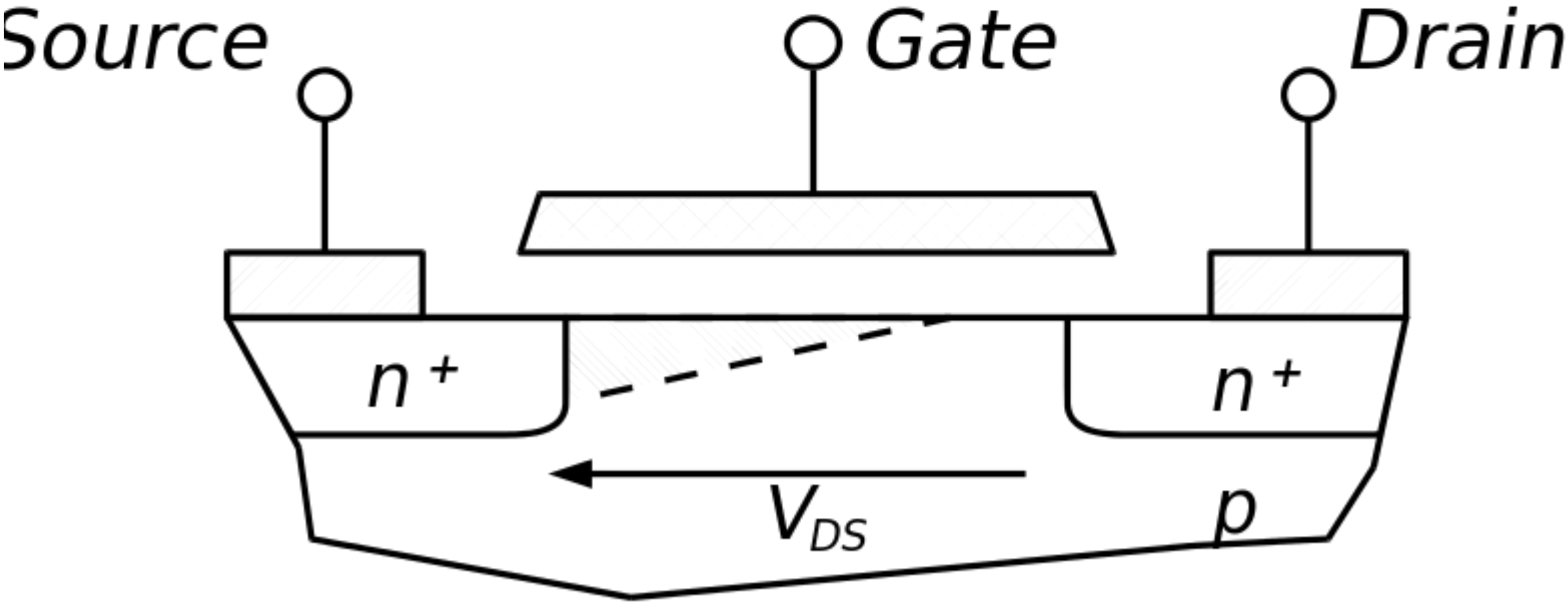
N-type MOSFET (Conducting)



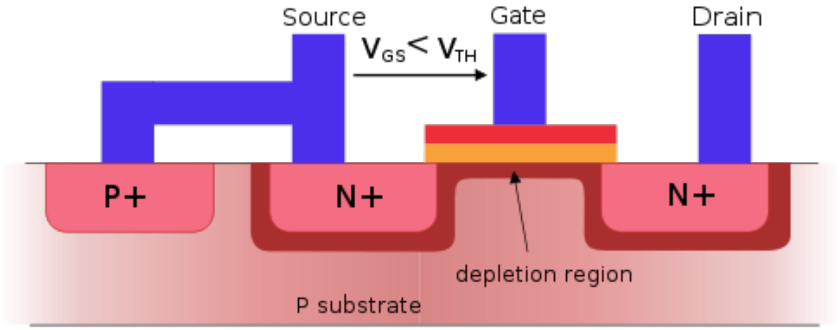
N-type MOSFET (Conducting)

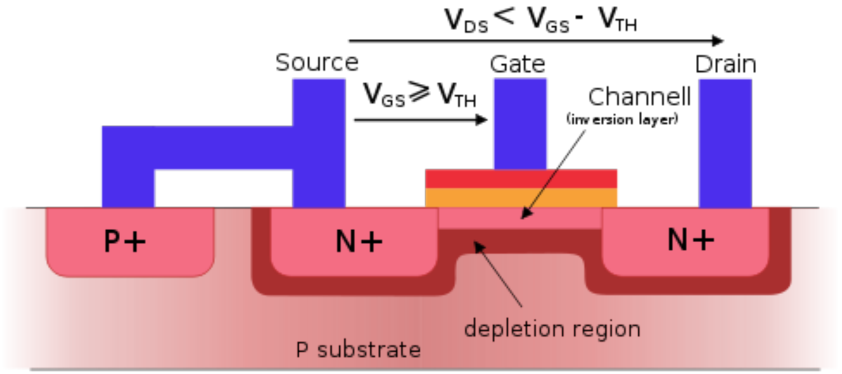


N-type MOSFET (pinchoff)

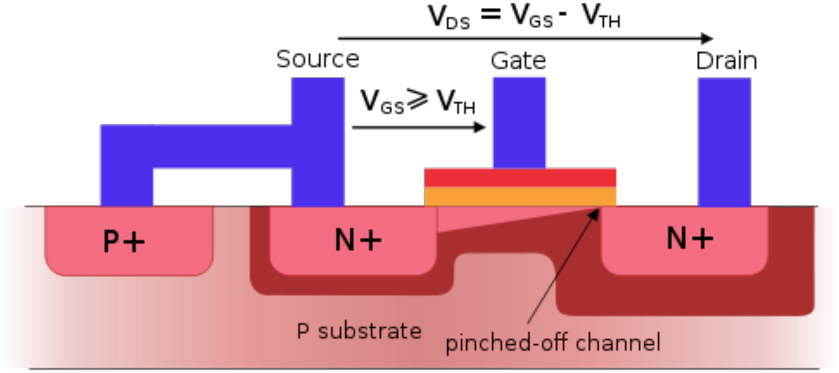


Different modes of operation

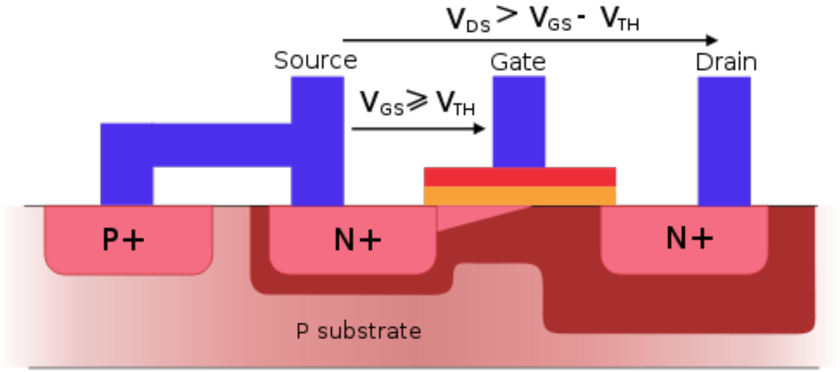




Linear operating region (ohmic mode)

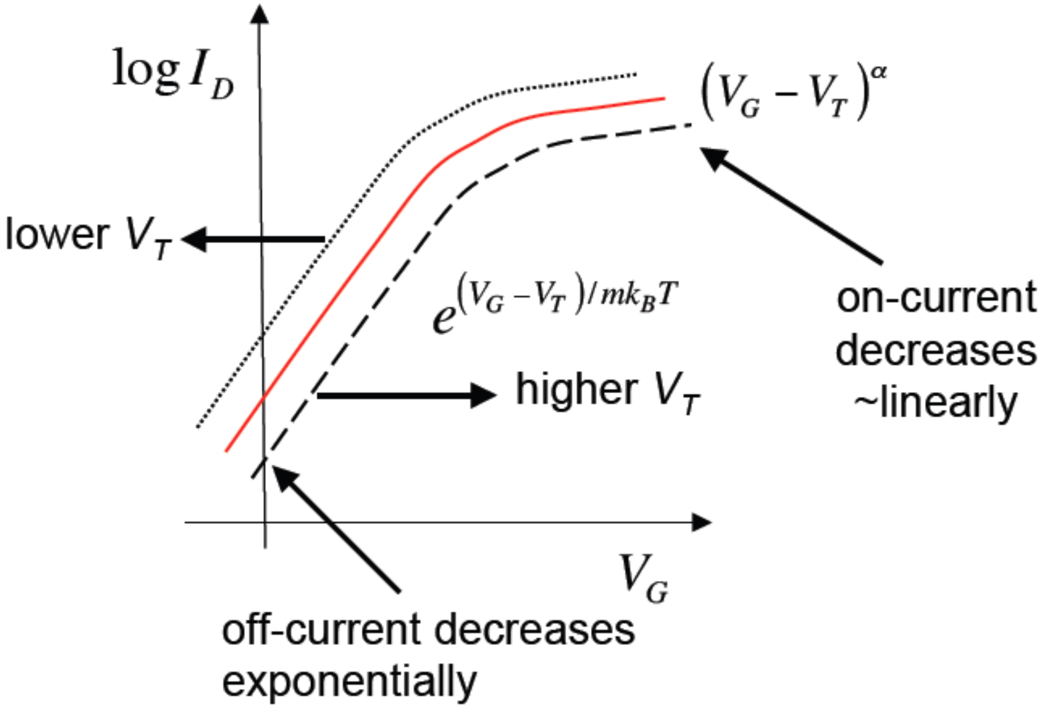


Saturation mode at point of pinch-off



Saturation mode

Threshhold Voltage



lower V_T

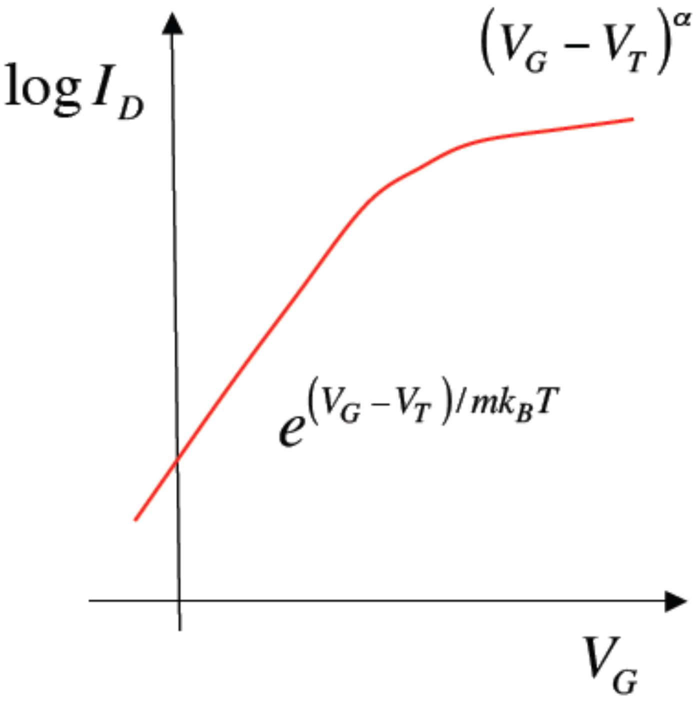
higher V_T

on-current decreases ~linearly

off-current decreases exponentially

Lundstrom EE-612 F06

Threshhold Voltage



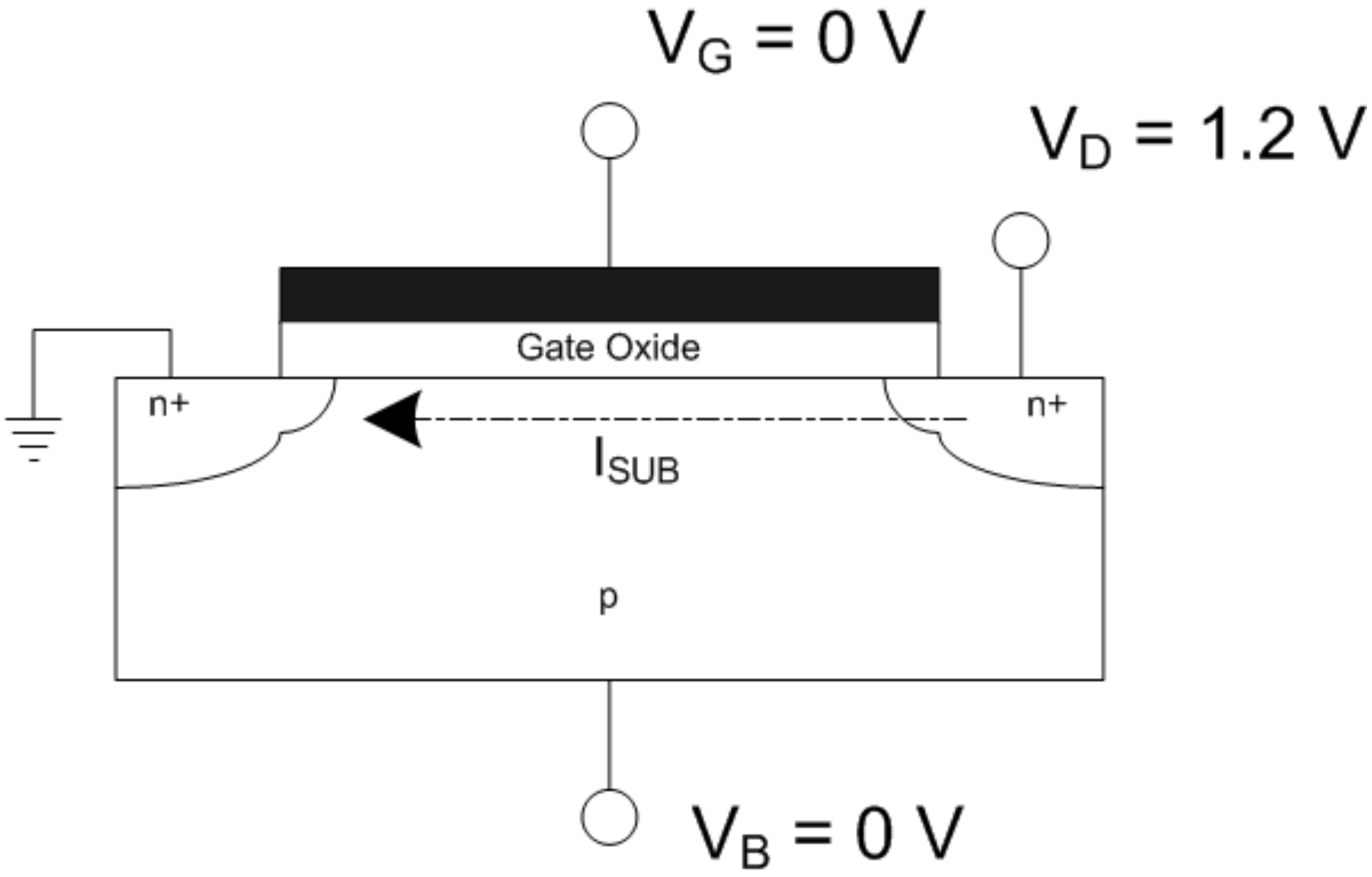
V_T selection is a trade-off between high on-current (low V_T) and low off-current (high V_T).

High-performance (high I_{ON}):
V_{DD} = 1.1V
V_T = 0.17V (15% of V_{DD})

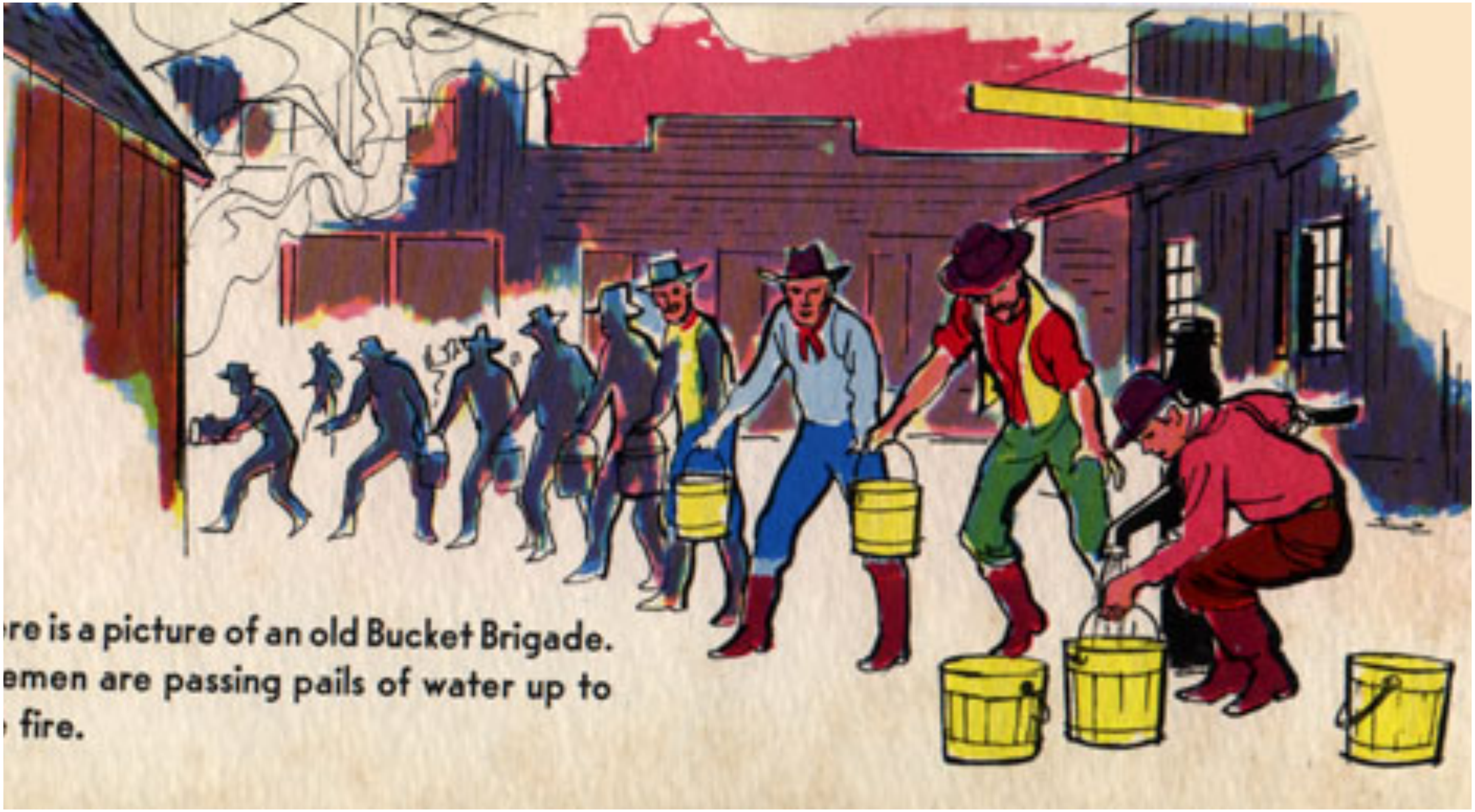
Low-power (low I_{OFF}):
V_{DD} = 1.2V
V_T =0.52V (43% of V_{DD})

60 nm node from ITRS 2005 Ed.

Subthreshold Leakage



Water Pressure Affects Results



re is a picture of an old Bucket Brigade.
emen are passing pails of water up to
fire.

Challenges to MOSFET size reduction

- **Higher subthreshold conduction**
- As MOSFET geometries shrink, the voltage that can be applied to the gate must be reduced to maintain reliability. To maintain performance, the threshold voltage of the MOSFET has to be reduced as well. As threshold voltage is reduced, the transistor cannot be switched from complete turn-off to complete turn-on with the limited voltage swing available; the circuit design is a compromise between strong current in the "on" case and low current in the "off" case, and the application determines whether to favor one over the other. Subthreshold leakage (including subthreshold conduction, gate-oxide leakage and reverse-biased junction leakage), which was ignored in the past, now can consume upwards of half of the total power consumption of modern high-performance VLSI chips.[32][33][34]

- **Increased gate-oxide leakage**
- The gate oxide, which serves as insulator between the gate and channel, should be made as thin as possible to increase the channel conductivity and performance when the transistor is on and to reduce subthreshold leakage when the transistor is off. However, with current gate oxides with a thickness of around 1.2 nm (which in silicon is ~5 atoms thick) the quantum mechanical phenomenon of electron tunneling occurs between the gate and channel, leading to increased power consumption.
- Silicon dioxide has traditionally been used as the gate insulator. Silicon dioxide however has a modest dielectric constant. Increasing the dielectric constant of the gate dielectric allows a thicker layer while maintaining a high capacitance (capacitance is proportional to dielectric constant and inversely proportional to dielectric thickness). All else equal, a higher dielectric thickness reduces the quantum tunneling current through the dielectric between the gate and the channel.
- Insulators that have a larger dielectric constant than silicon dioxide (referred to as high-k dielectrics), such as group IVb metal silicates e.g. hafnium and zirconium silicates and oxides are being used to reduce the gate leakage from the 45 nanometer technology node onwards.
- On the other hand, the barrier height of the new gate insulator is an important consideration; the difference in conduction band energy between the semiconductor and the dielectric (and the corresponding difference in valence band energy) also affects leakage current level. For the traditional gate oxide, silicon dioxide, the former barrier is approximately 8 eV. For many alternative dielectrics the value is significantly lower, tending to increase the tunneling current, somewhat negating the advantage of higher dielectric constant.
- The maximum gate-source voltage is determined by the strength of the electric field able to be sustained by the gate dielectric before significant leakage occurs. As the insulating dielectric is made thinner, the electric field strength within it goes up for a fixed voltage. This necessitates using lower voltages with the thinner dielectric.

- .

Challenges to MOSFET size reduction

- **Increased junction leakage**
- To make devices smaller, junction design has become more complex, leading to higher doping levels, shallower junctions, "halo" doping and so forth,[35][36] all to decrease drain-induced barrier lowering (see the section on junction design). To keep these complex junctions in place, the annealing steps formerly used to remove damage and electrically active defects must be curtailed[37] increasing junction leakage. Heavier doping is also associated with thinner depletion layers and more recombination centers that result in increased leakage current, even without lattice damage.

- **Lower output resistance**
- For analog operation, good gain requires a high MOSFET output impedance, which is to say, the MOSFET current should vary only slightly with the applied drain-to-source voltage. As devices are made smaller, the influence of the drain competes more successfully with that of the gate due to the growing proximity of these two electrodes, increasing the sensitivity of the MOSFET current to the drain voltage. To counteract the resulting decrease in output resistance, circuits are made more complex, either by requiring more devices, for example the cascode and cascade amplifiers, or by feedback circuitry using operational amplifiers.

- **Lower transconductance**
- The transconductance of the MOSFET decides its gain and is proportional to hole or electron mobility (depending on device type), at least for low drain voltages. As MOSFET size is reduced, the fields in the channel increase and the dopant impurity levels increase. Both changes reduce the carrier mobility, and hence the transconductance. As channel lengths are reduced without proportional reduction in drain voltage, raising the electric field in the channel, the result is velocity saturation of the carriers, limiting the current and the transconductance.

- **Interconnect capacitance**
- Traditionally, switching time was roughly proportional to the gate capacitance of gates. However, with transistors becoming smaller and more transistors being placed on the chip, interconnect capacitance (the capacitance of the metal-layer connections between different parts of the chip) is becoming a large percentage of capacitance.[38] [39] Signals have to travel through the interconnect, which leads to increased delay and lower performance.

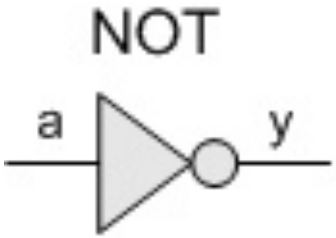
Challenges to MOSFET size reduction

- **Heat production**
- The ever-increasing density of MOSFETs on an integrated circuit creates problems of substantial localized heat generation that can impair circuit operation. Circuits operate more slowly at high temperatures, and have reduced reliability and shorter lifetimes. Heat sinks and other cooling devices and methods are now required for many integrated circuits including microprocessors.

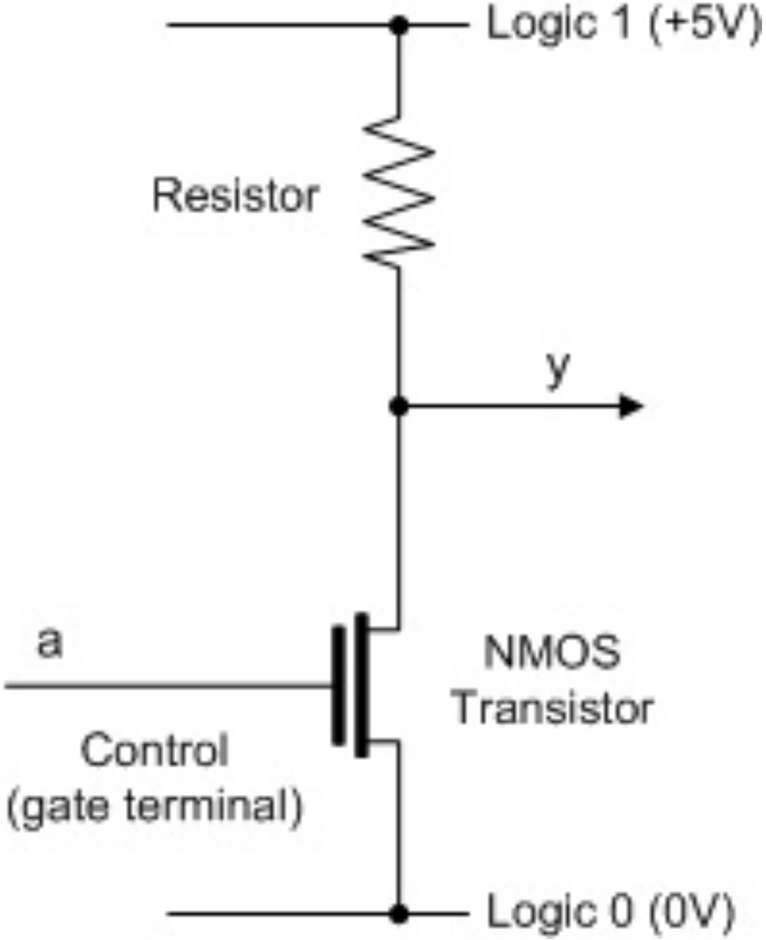
- **Process variations**
- With MOSFETS becoming smaller, the number of atoms in the silicon that produce many of the transistor's properties is becoming fewer, with the result that control of dopant numbers and placement is more erratic. During chip manufacturing, random process variations affect all transistor dimensions: length, width, junction depths, oxide thickness *etc.*, and become a greater percentage of overall transistor size as the transistor shrinks. The transistor characteristics become less certain, more statistical. The random nature of manufacture means we do not know which particular example MOSFETs actually will end up in a particular instance of the circuit. This uncertainty forces a less optimal design because the design must work for a great variety of possible component MOSFETs. See process variation, design for manufacturability, reliability engineering, and statistical process control.[40]

- **Modeling challenges**
- Modern ICs are computer-simulated with the goal of obtaining working circuits from the very first manufactured lot. As devices are miniaturized, the complexity of the processing makes it difficult to predict exactly what the final devices look like, and modeling of physical processes becomes more challenging as well. In addition, microscopic variations in structure due simply to the probabilistic nature of atomic processes require statistical (not just deterministic) predictions. These factors combine to make adequate simulation and "right the first time" manufacture difficult

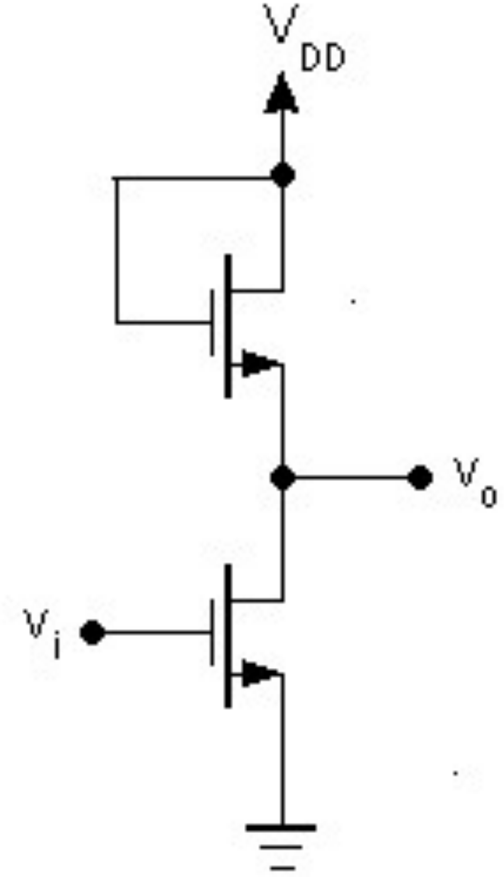
NMOS Inverter



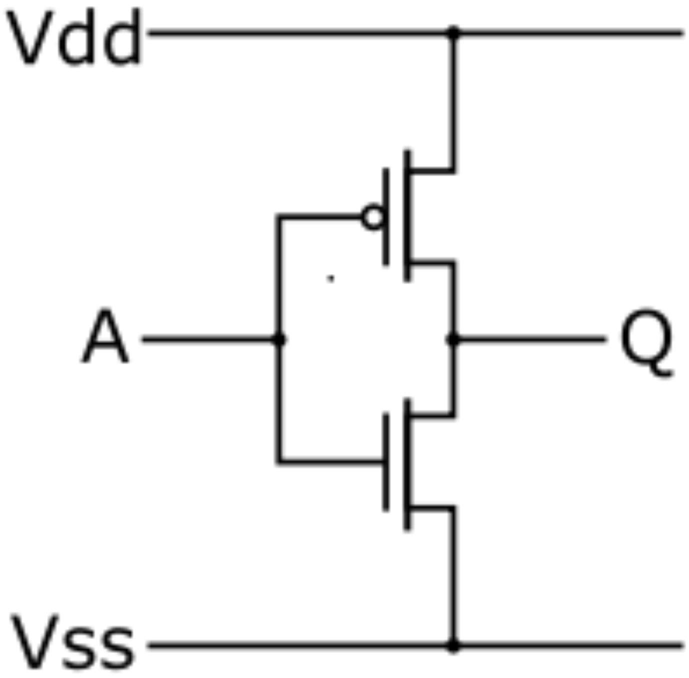
a	y
0	1
1	0



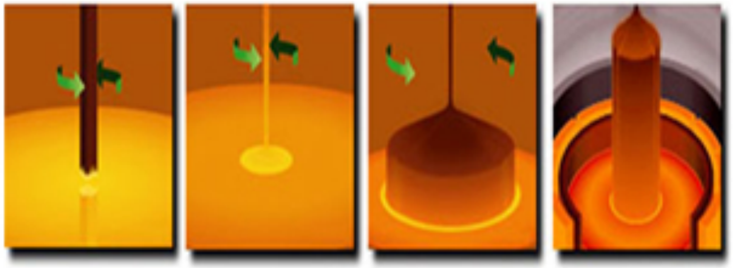
NMOS Inverter

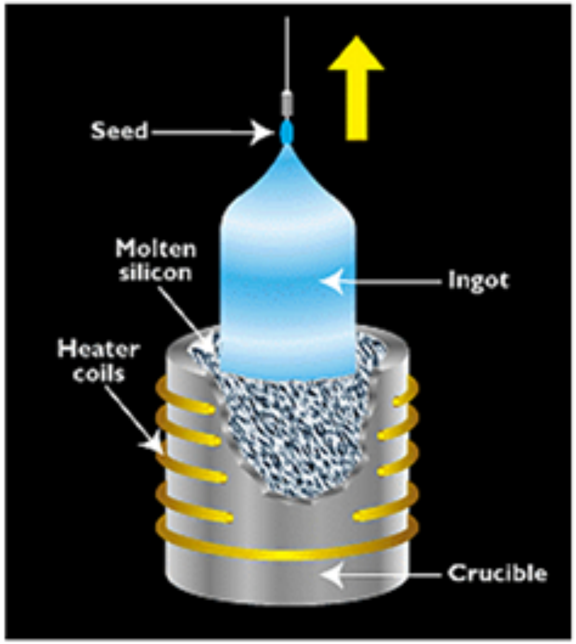


CMOS Inverter



Silicon Ingots





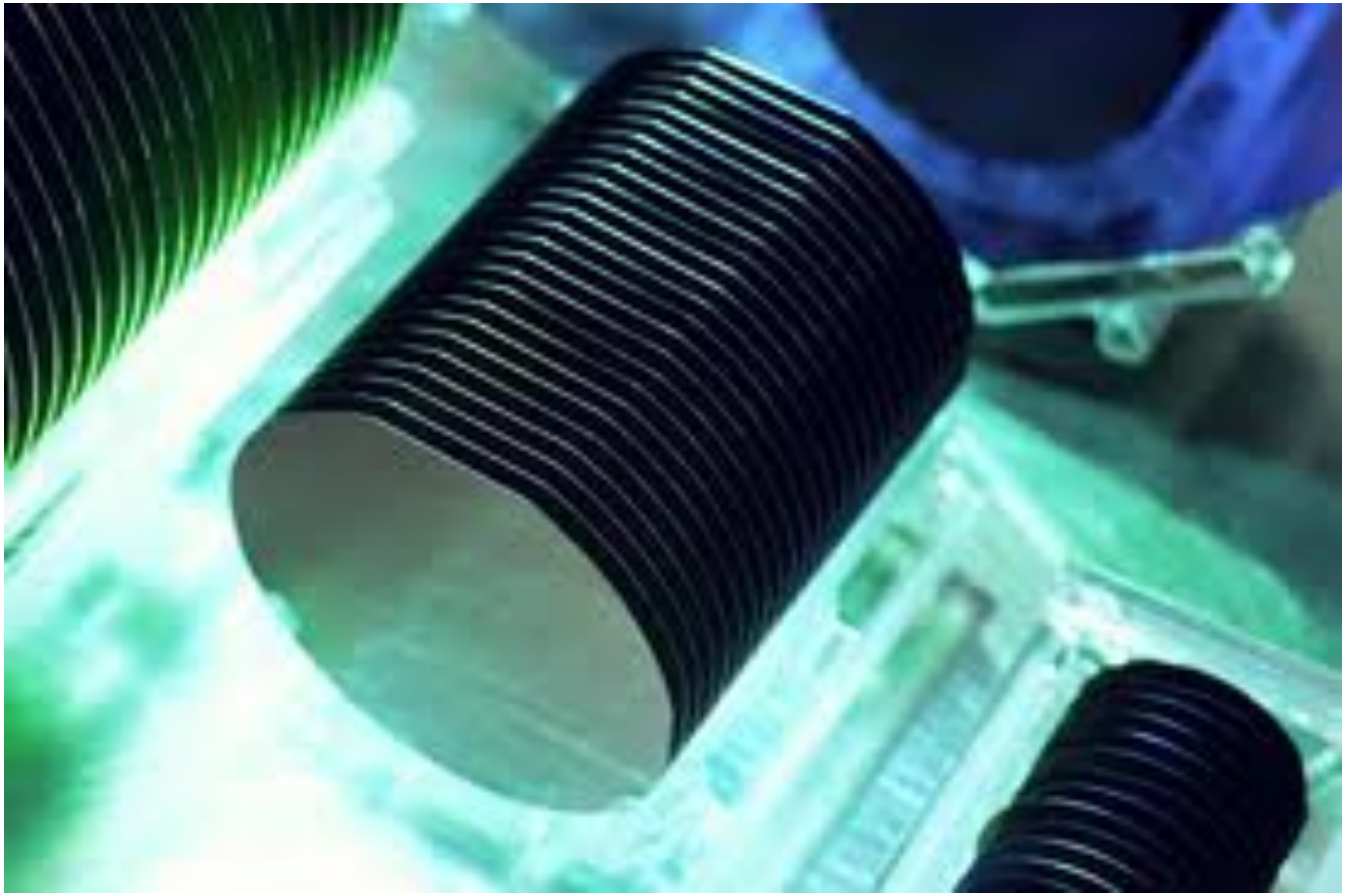
Silicon Ingot

Silicon Ingot

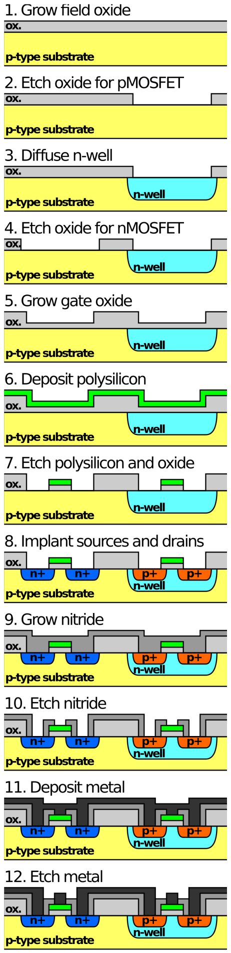
Creating Silicon Wafers

Creating Silicon Wafers

Silicon Wafers



Fabrication



1. Grow field oxide

2. Etch oxide for pMOSFET

3. Diffuse n-well

4. Etch oxide for nMOSFET

5. Grow gate oxide

6. Deposit polysilicon

7. Etch polysilicon and oxide

8. Implant sources and drains

9. Grow nitride

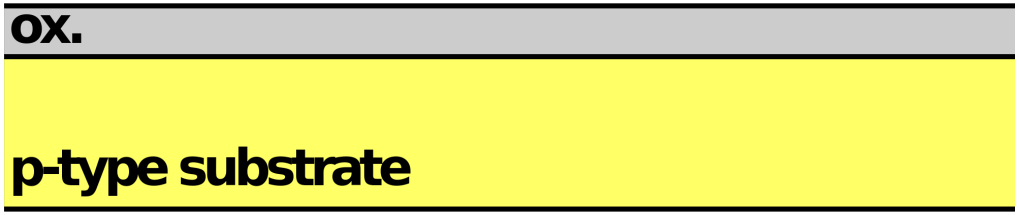
10. Etch nitride

11. Deposit metal

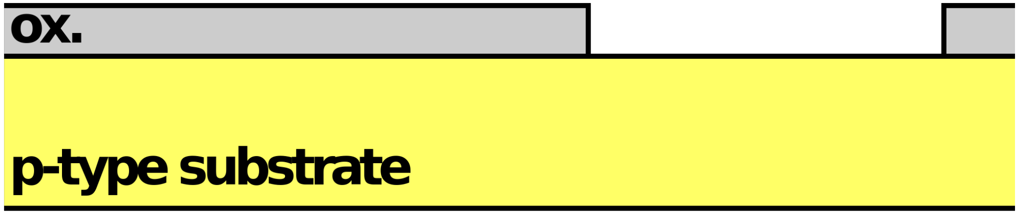
12. Etch metal

Fabrication 1-3

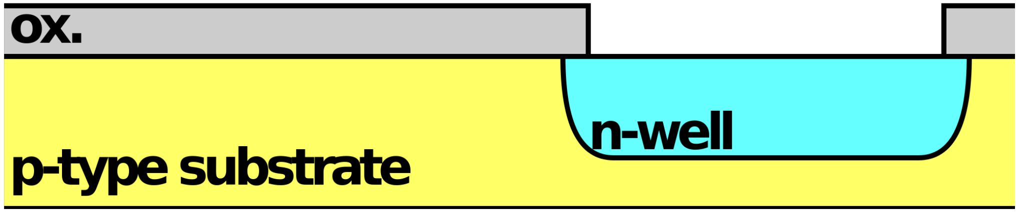
1. Grow field oxide



2. Etch oxide for pMOSFET



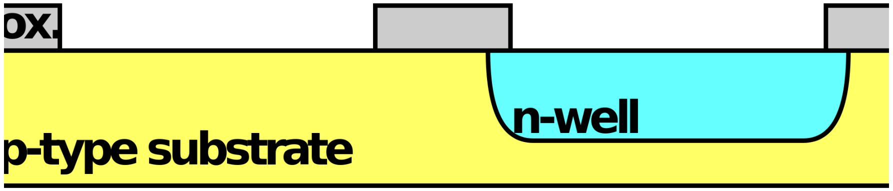
3. Diffuse n-well



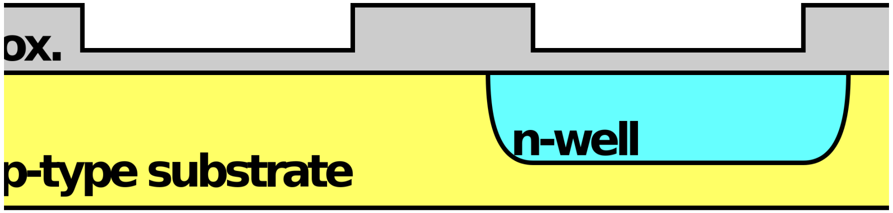
Fabrication 4-6

---

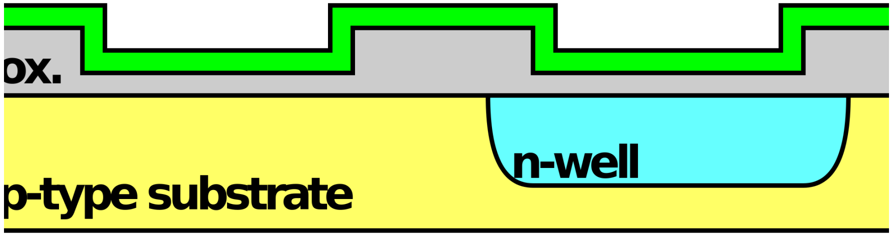
4. Etch oxide for nMOSFET



5. Grow gate oxide

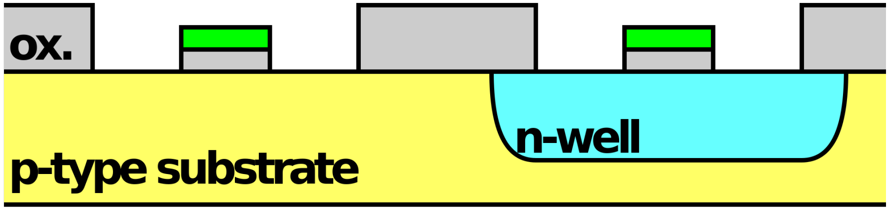


6. Deposit polysilicon

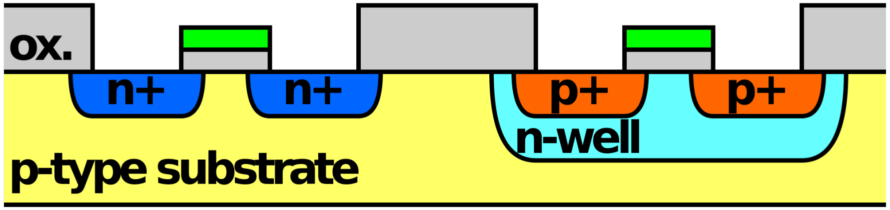


Fabrication 7-9

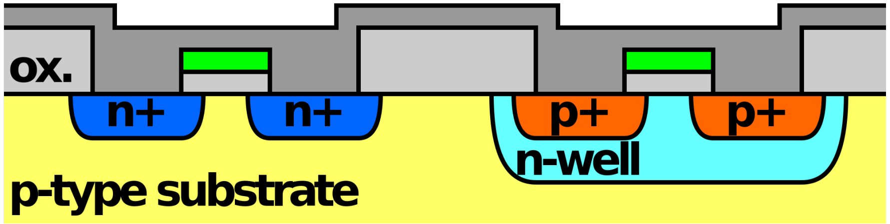
7. Etch polysilicon and oxide



8. Implant sources and drains

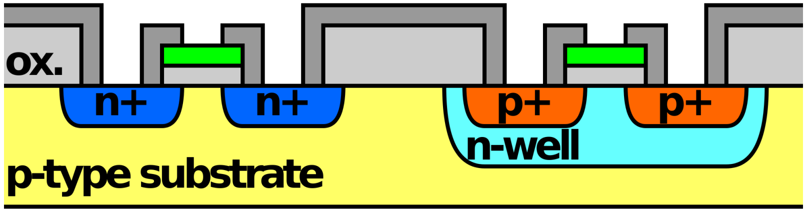


9. Grow nitride

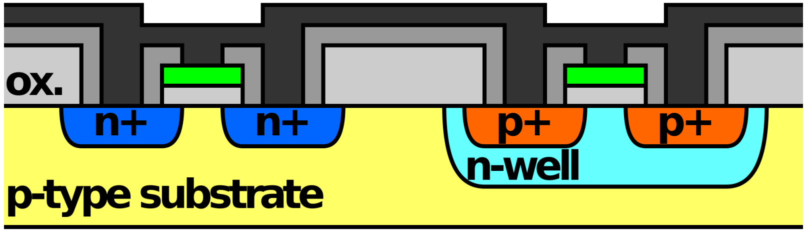


Fabrication 10-12

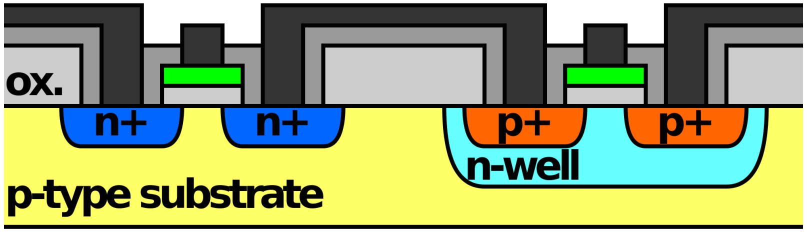
10. Etch nitride



11. Deposit metal

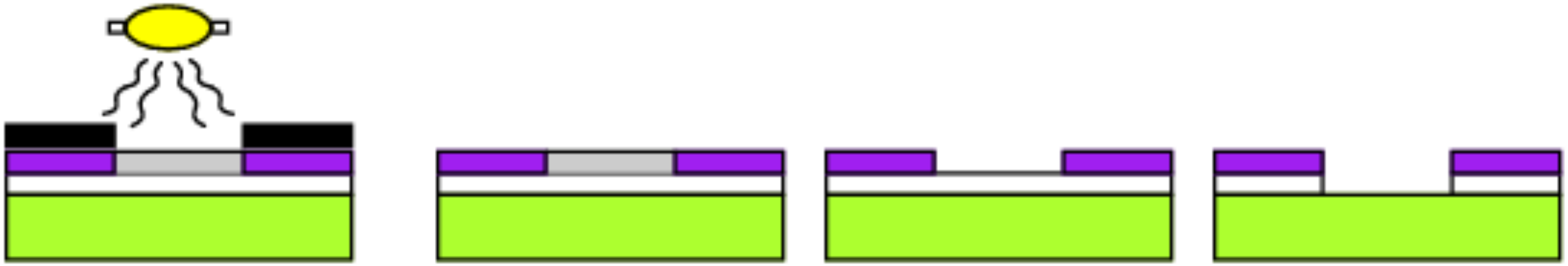


12. Etch metal



Fabrication Steps

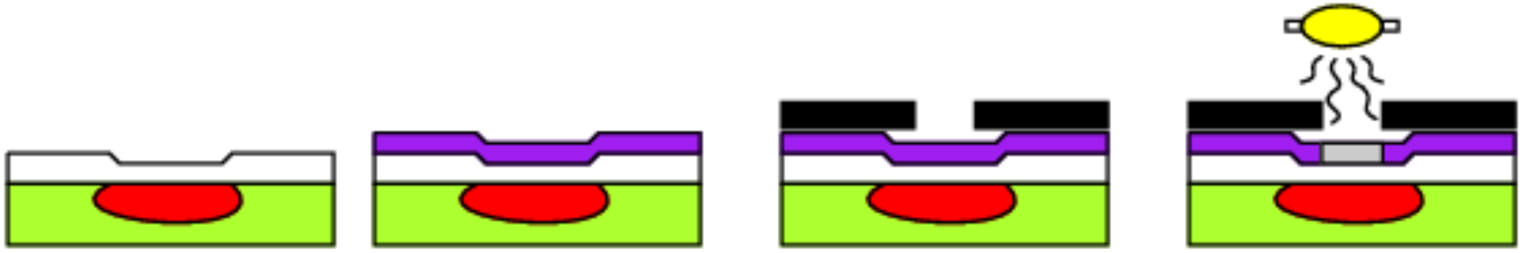
(a) N-type wafer (b) grow SiO_2 (c) apply photoresist (d) place mask



(e) expose (f) remove mask (g) develop resist (h) HF etch

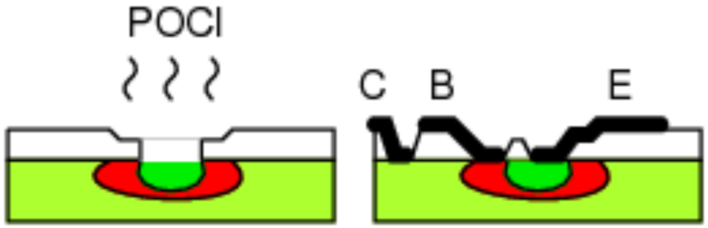
(i) strip resist (j) P-type diffusion

Fabrication Steps



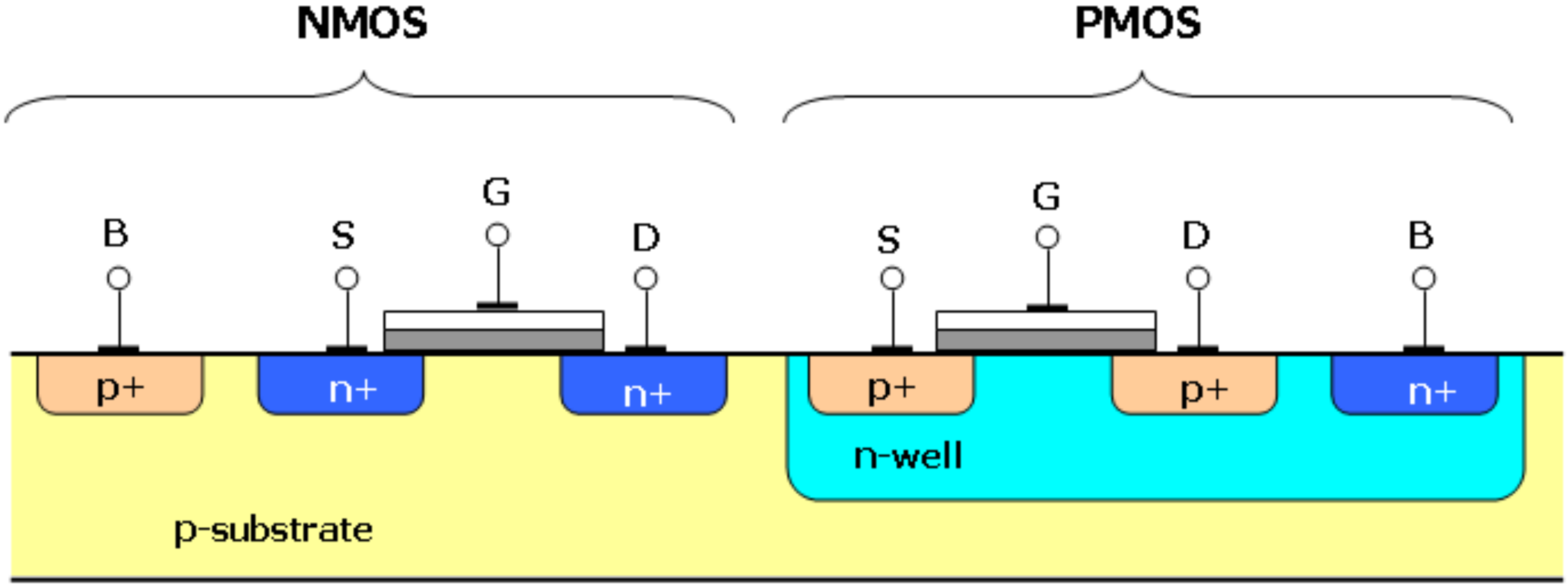
(k) grow SiO_2 (l) apply photoresist (m) place mask (n) expose

(o) remove mask (p) develop resist (q) HF etch (r) strip resist

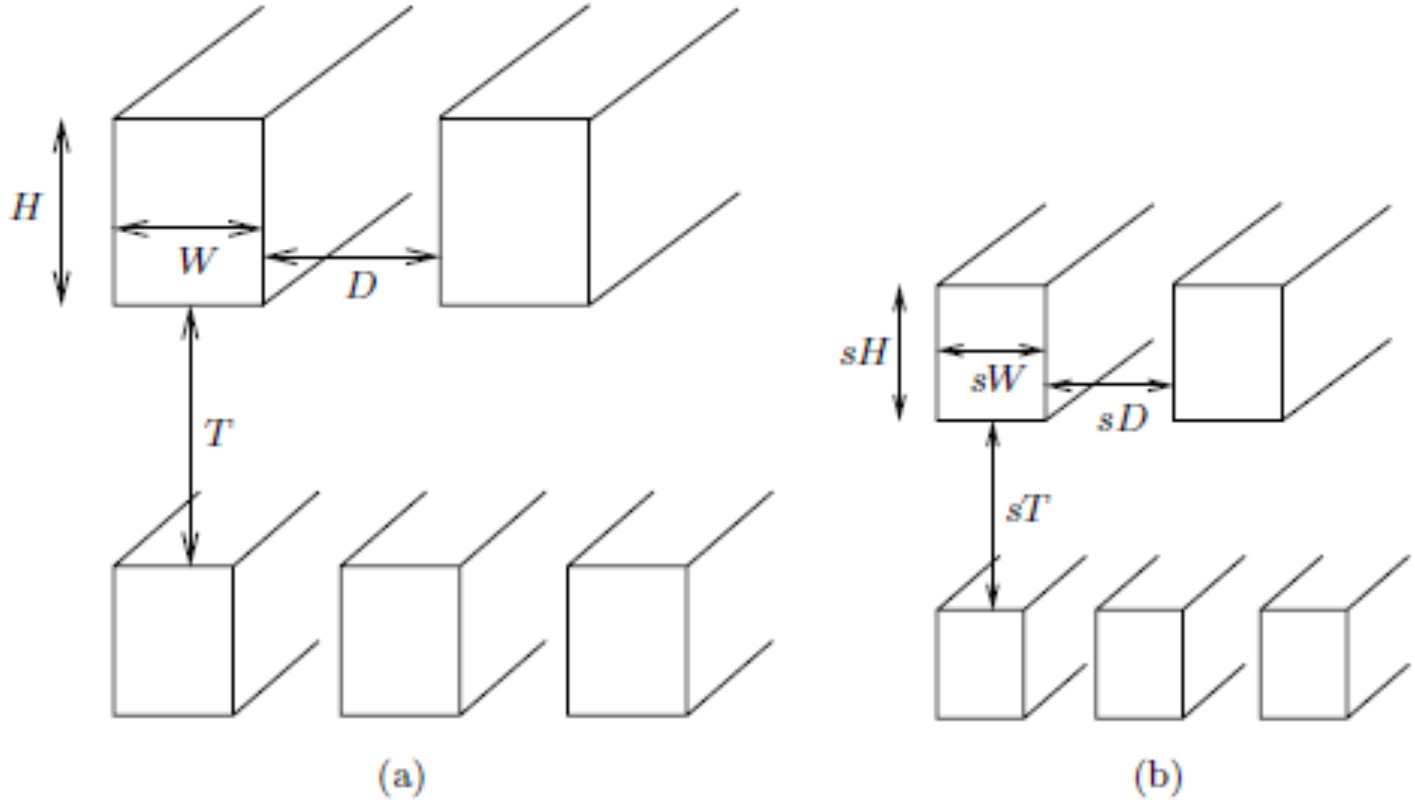


(s) N-type diffusion (t) metalization

NMOS and PMOS devices



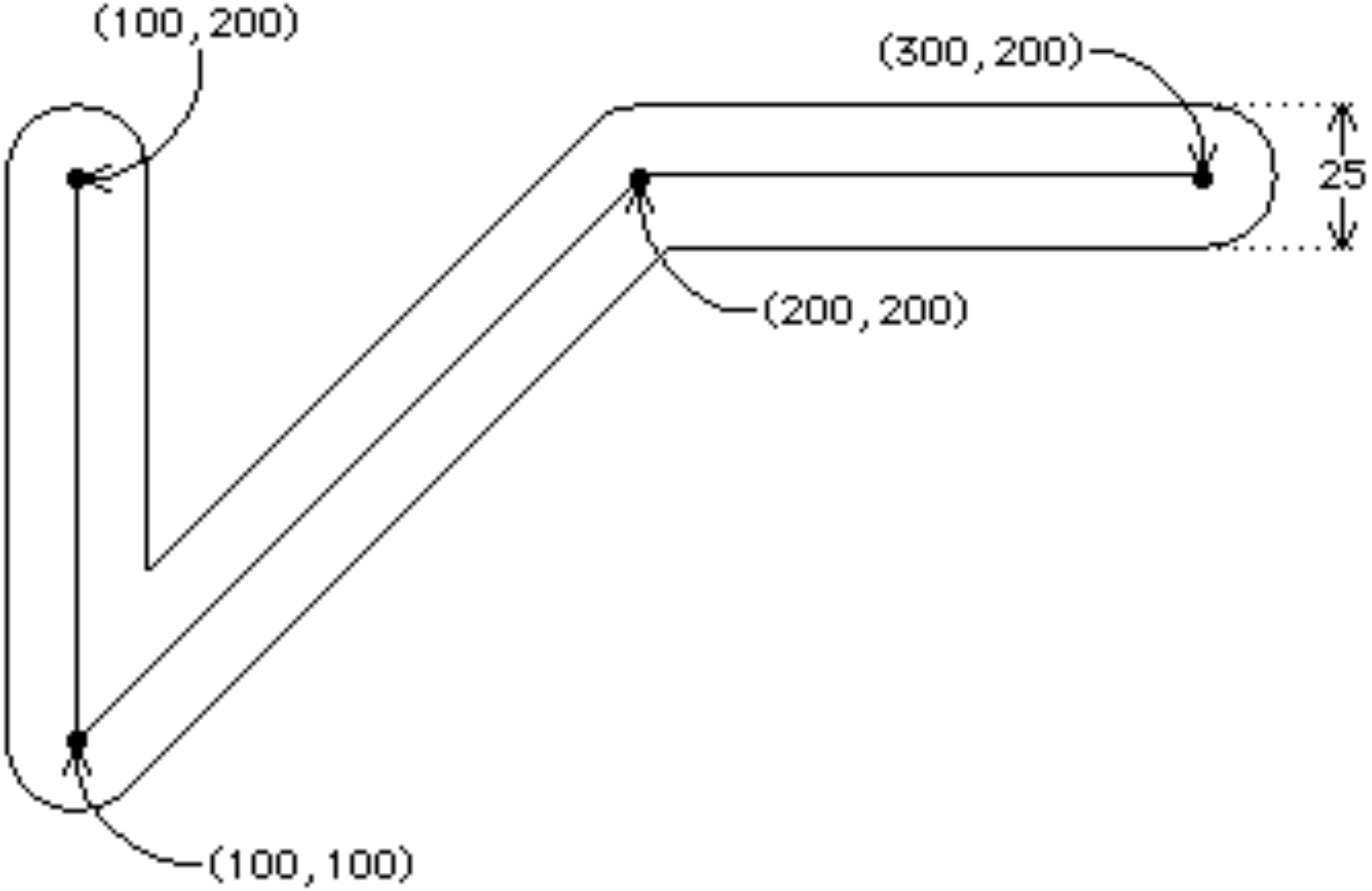
Wires and Scaling



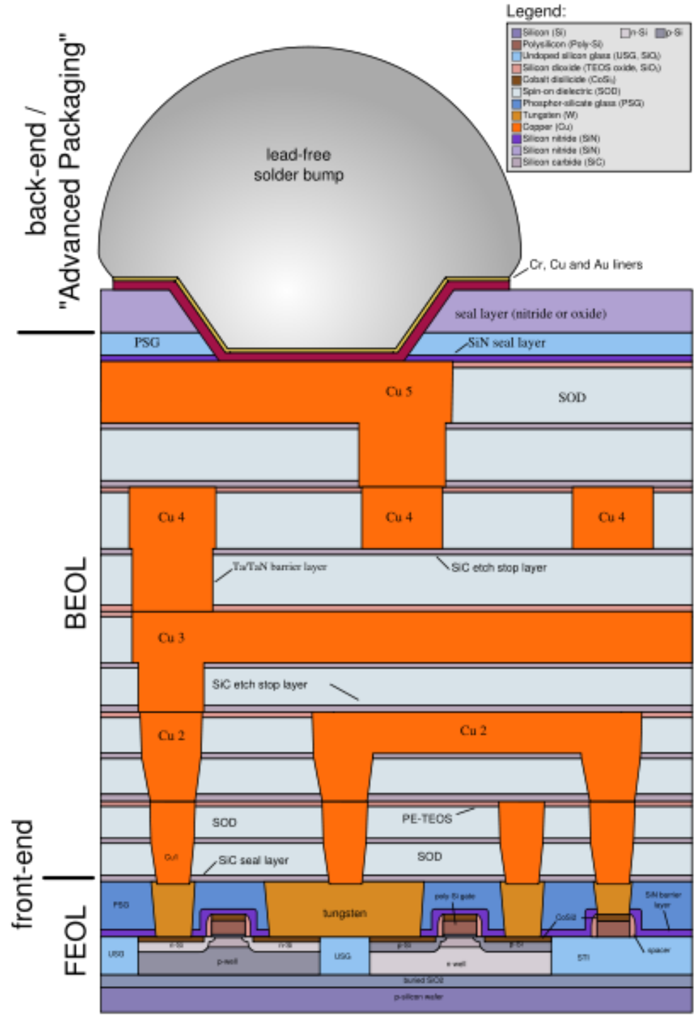
(a) (b)

Fig. 1.9. (a) Interconnects in a given process technology. (b) Ideally scaled interconnects in the next process generation.

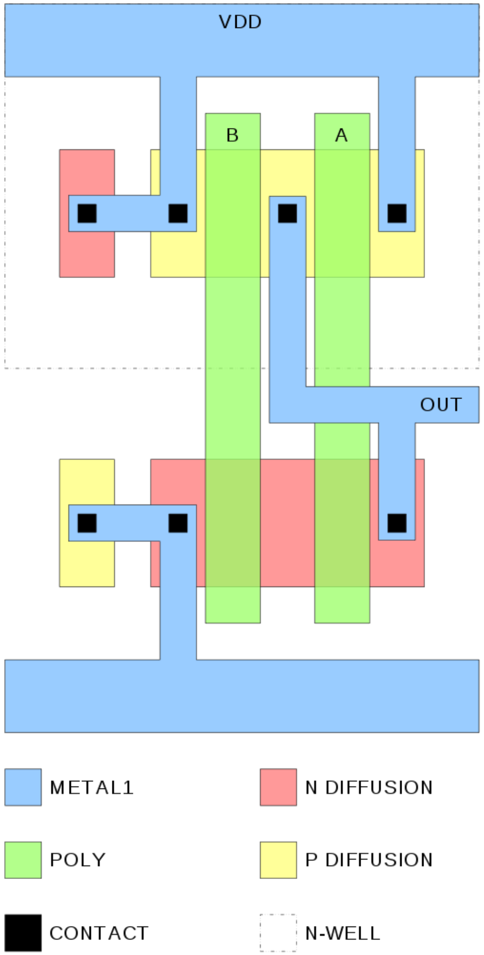
Feature Layout



Cross-section of Final Product

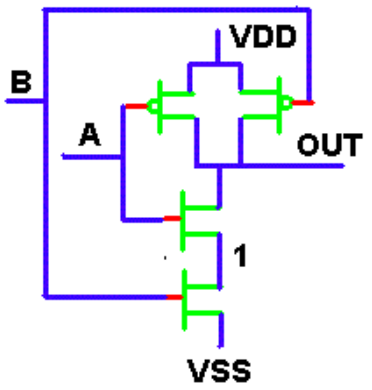


VLSI Layout


VDD
B
A
OUT
METAL1
N DIFFUSION
POLY
P DIFFUSION
CONTACT
N-WELL

VLSI Layout of NAND Gate

TWO INPUT NAND GATE

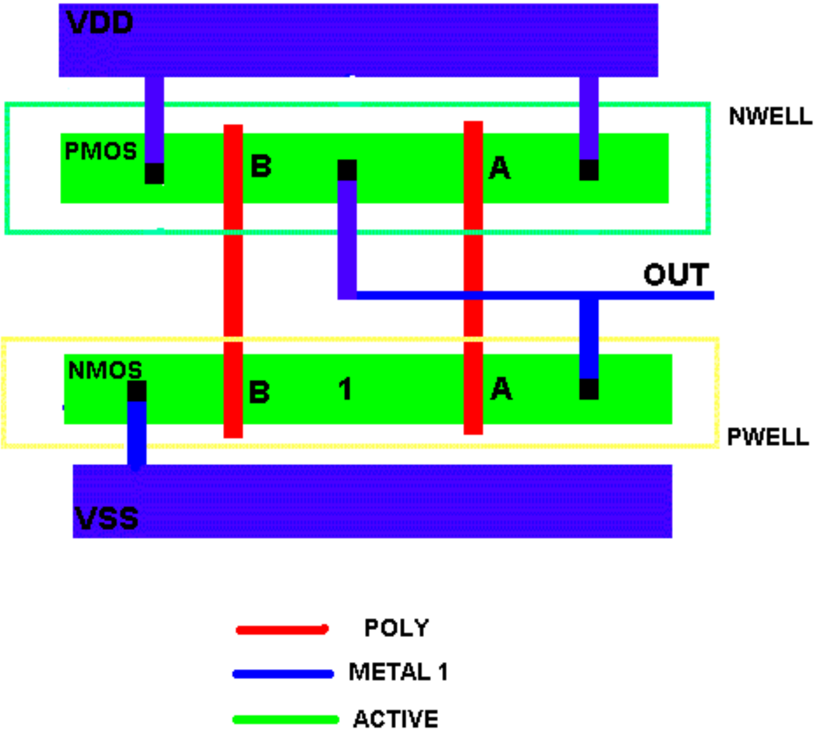


MINIMUM SIZE GATE

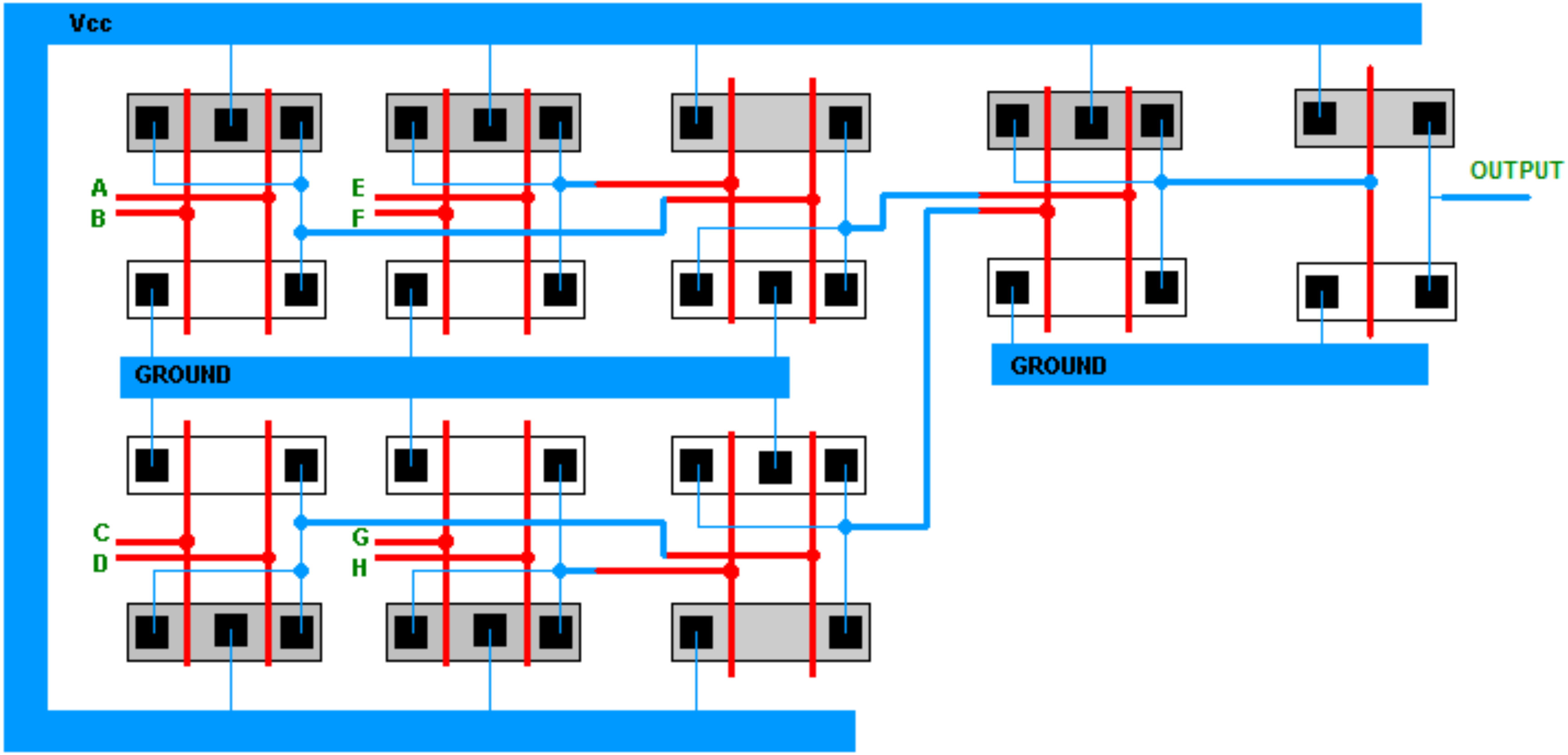
LENGTH = 2
WIDTH = 4

SIZED GATES

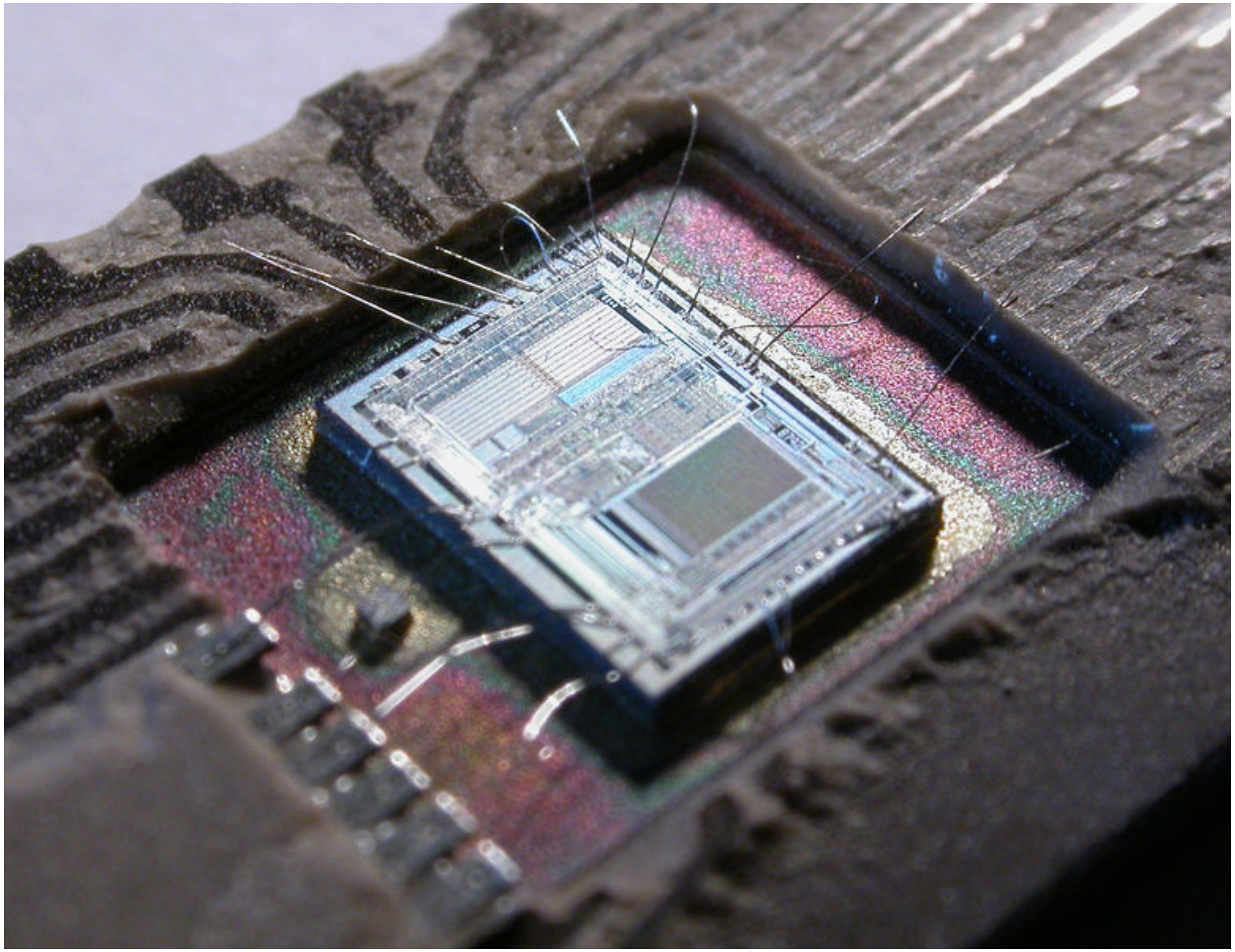
NMOS	PMOS
$\frac{W}{L}$ $\frac{8}{2}$	$\frac{W}{L}$ $\frac{12}{2}$



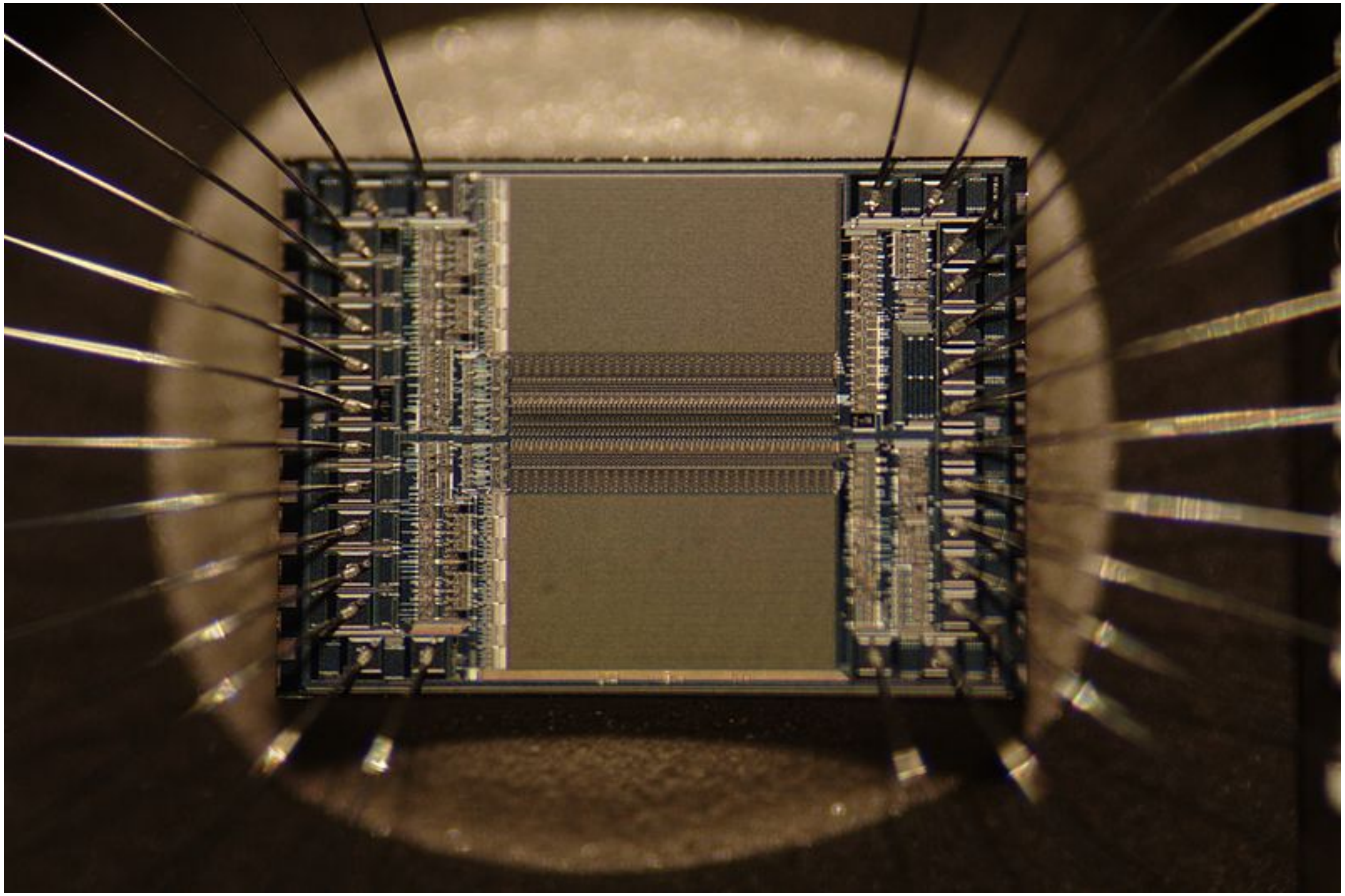
8-input Device



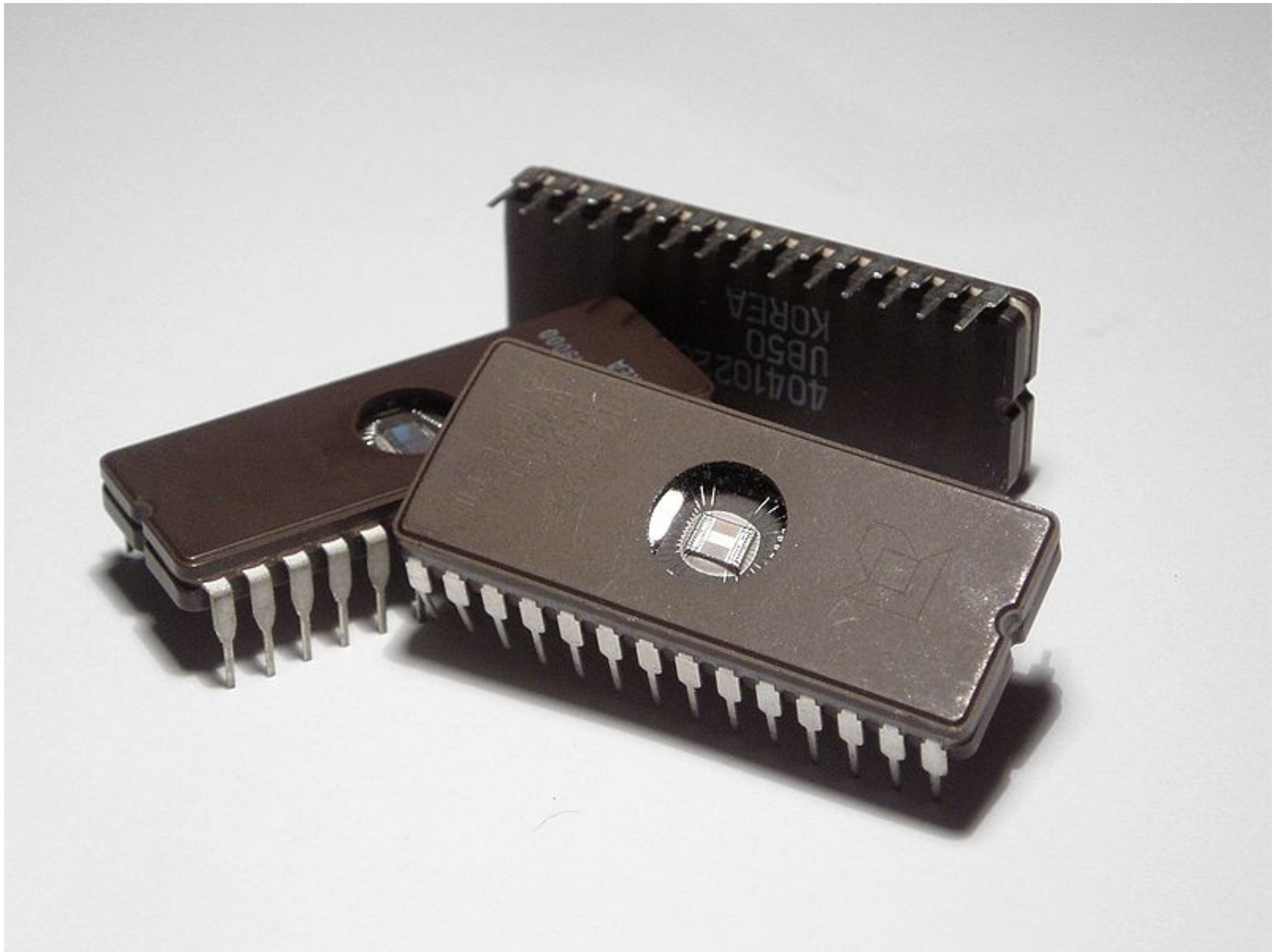
Die and External Connections



Die with Active Circuits, I/O



EPROM



Some Circuits