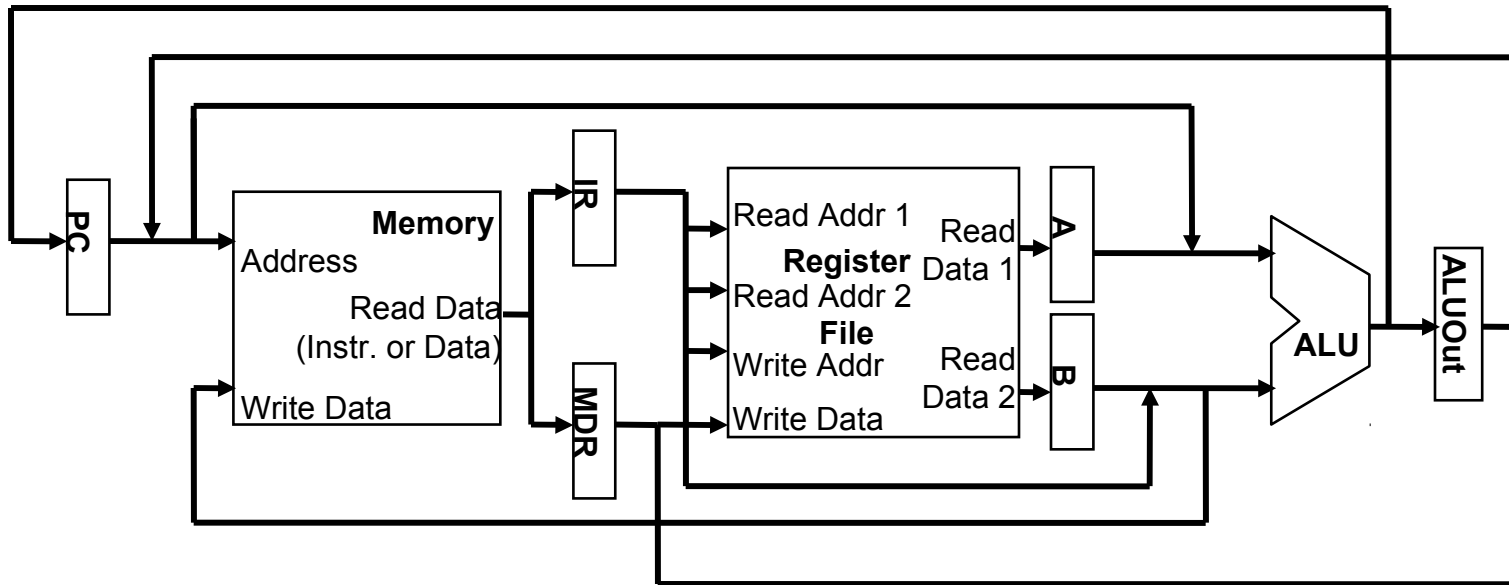


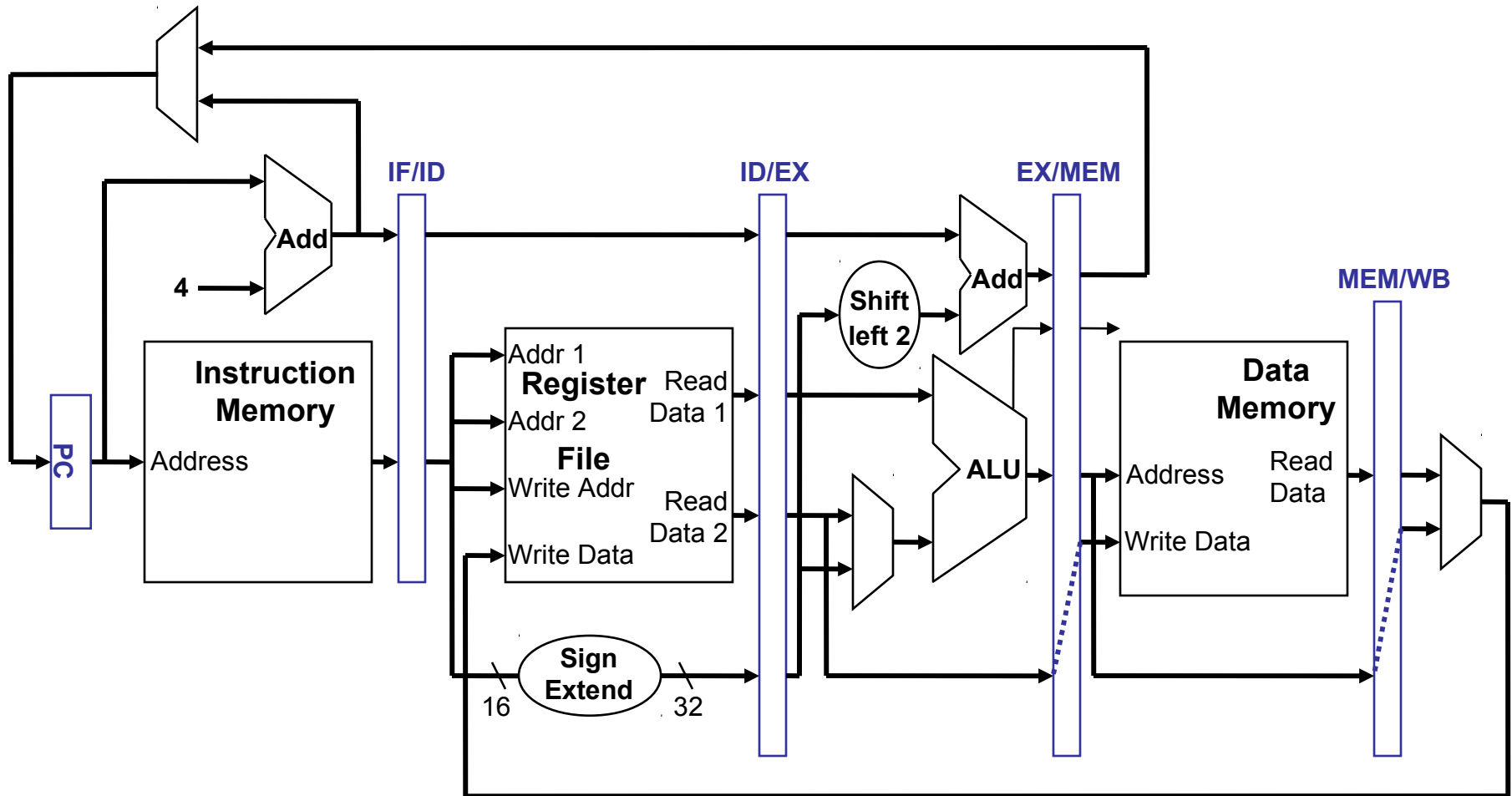
# Multicycle design

---

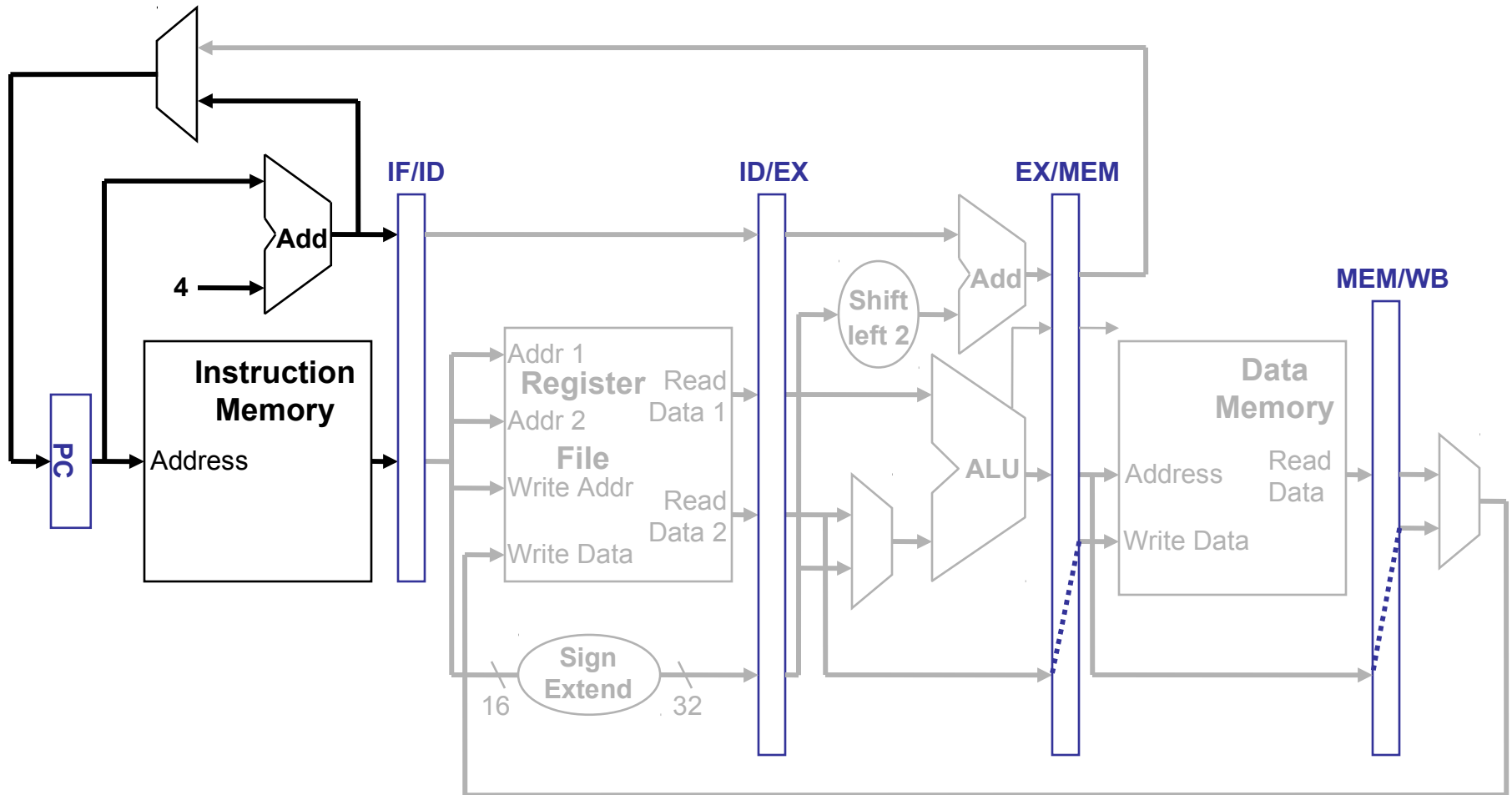


# Pipelined State Registers

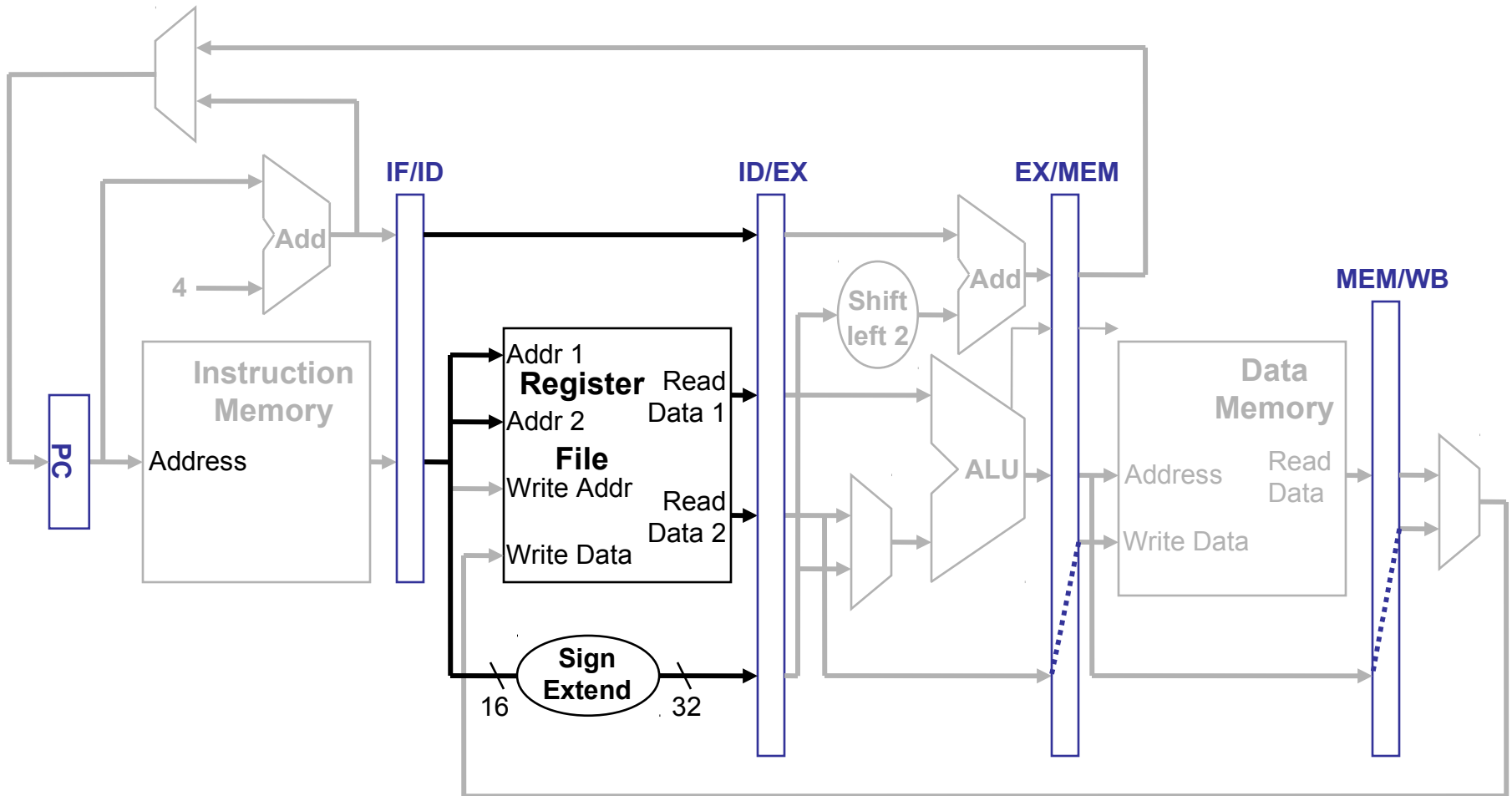
- More registers necessary for a pipelined CPU



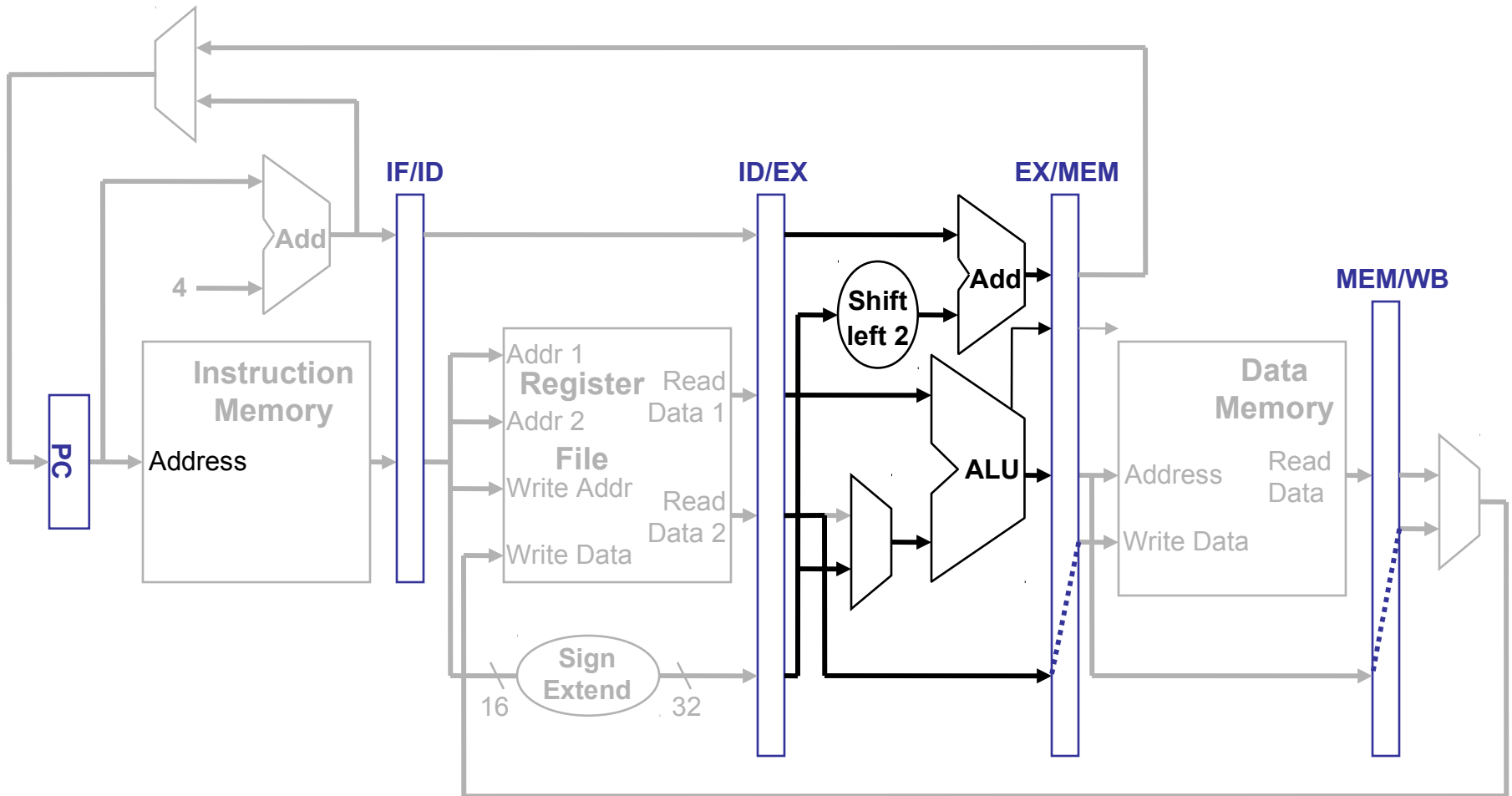
# Load Word Example (Fetch)



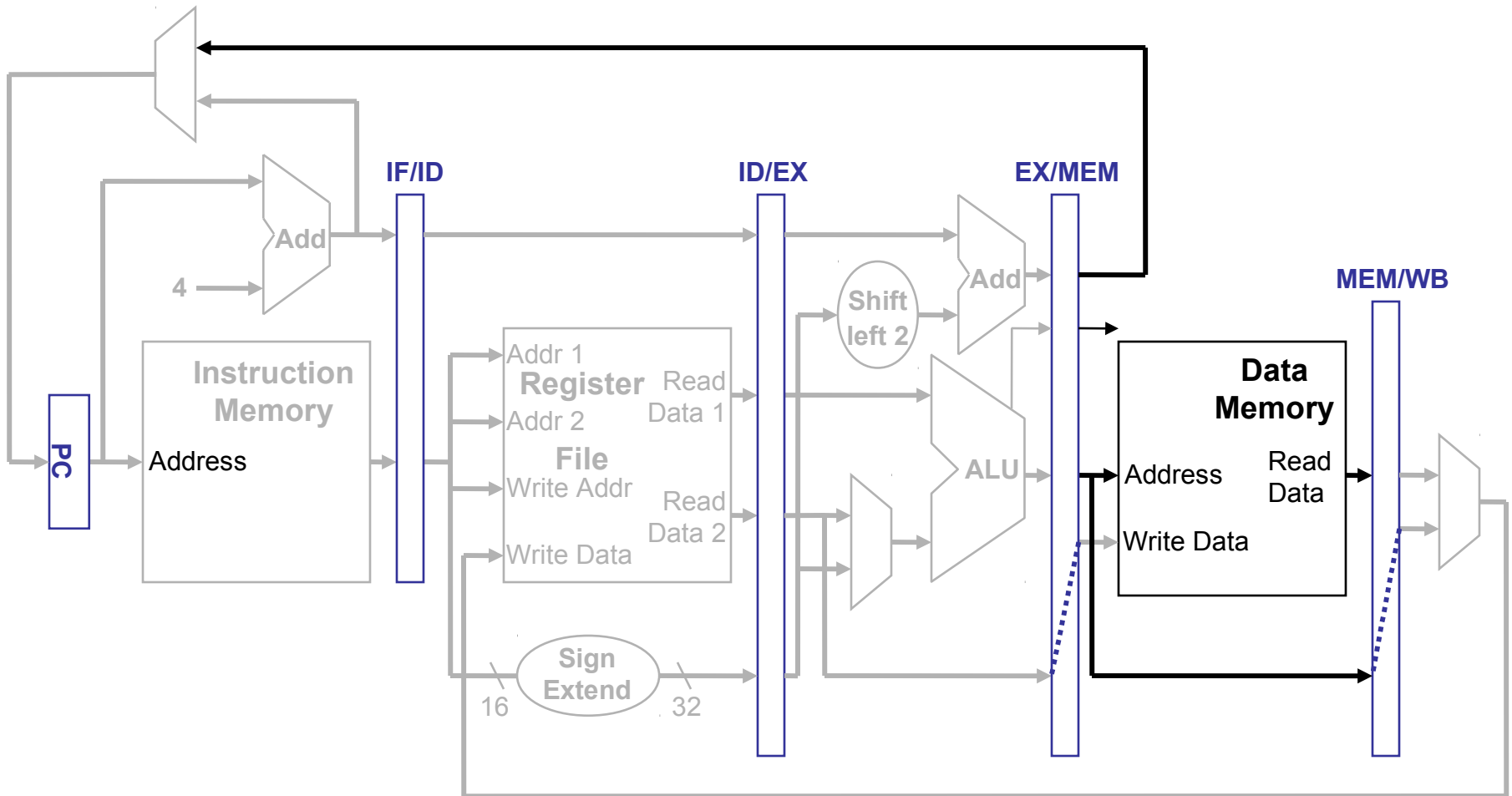
# Load Word Example (Decode)



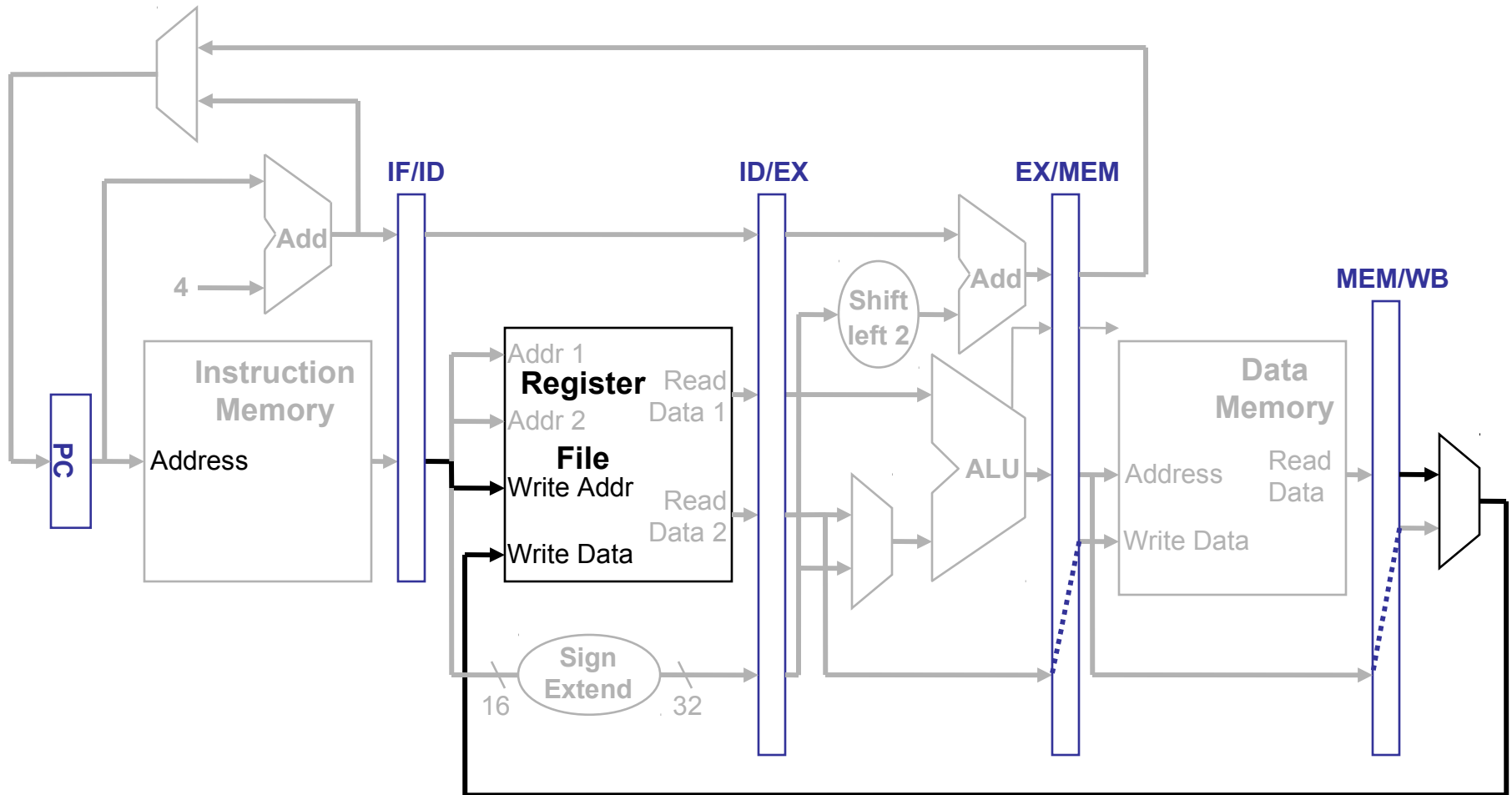
# Load Word Example (Execute)



# Load Word Example (Memory)

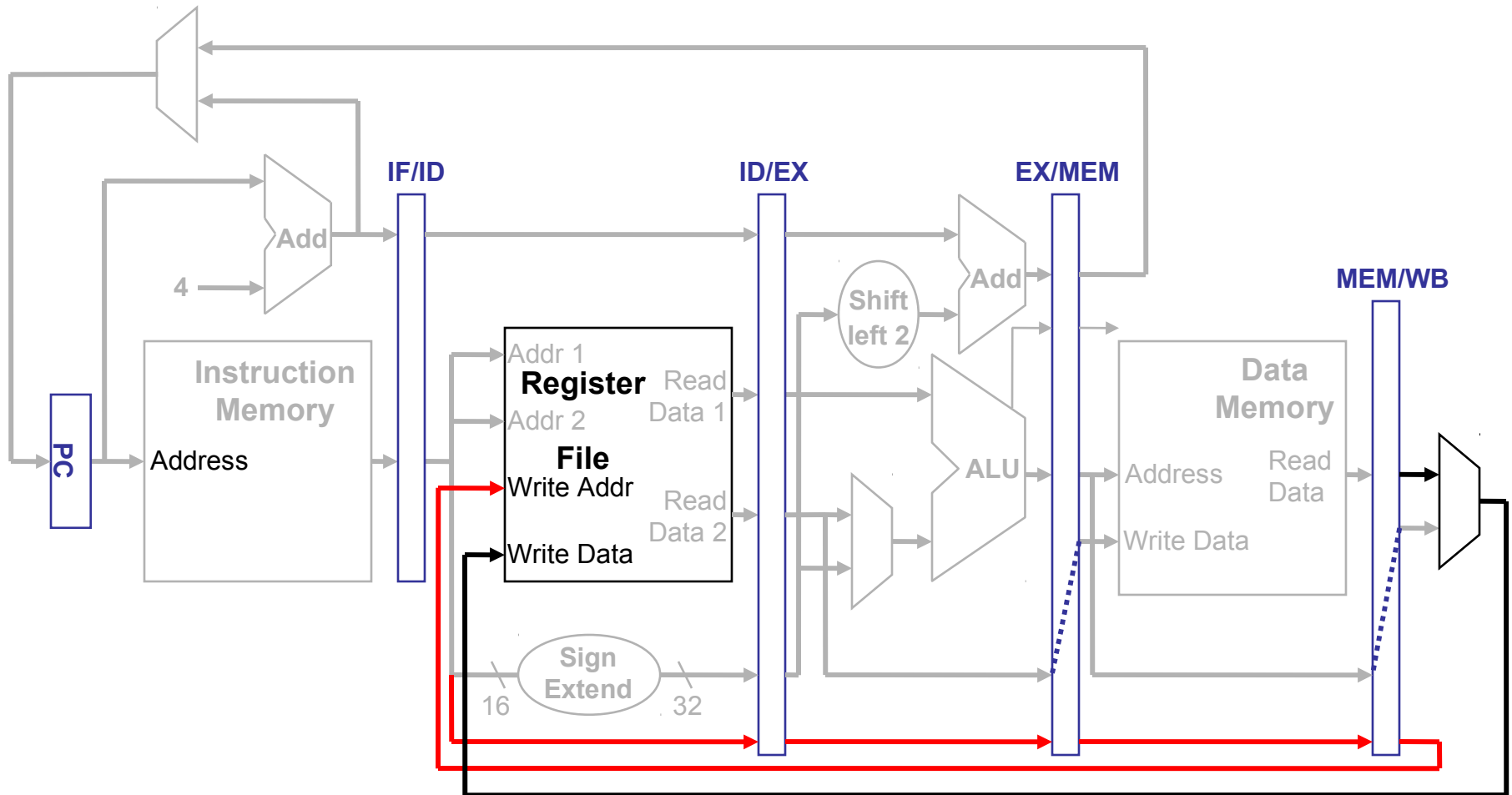


# Load Word Example (Write Back)



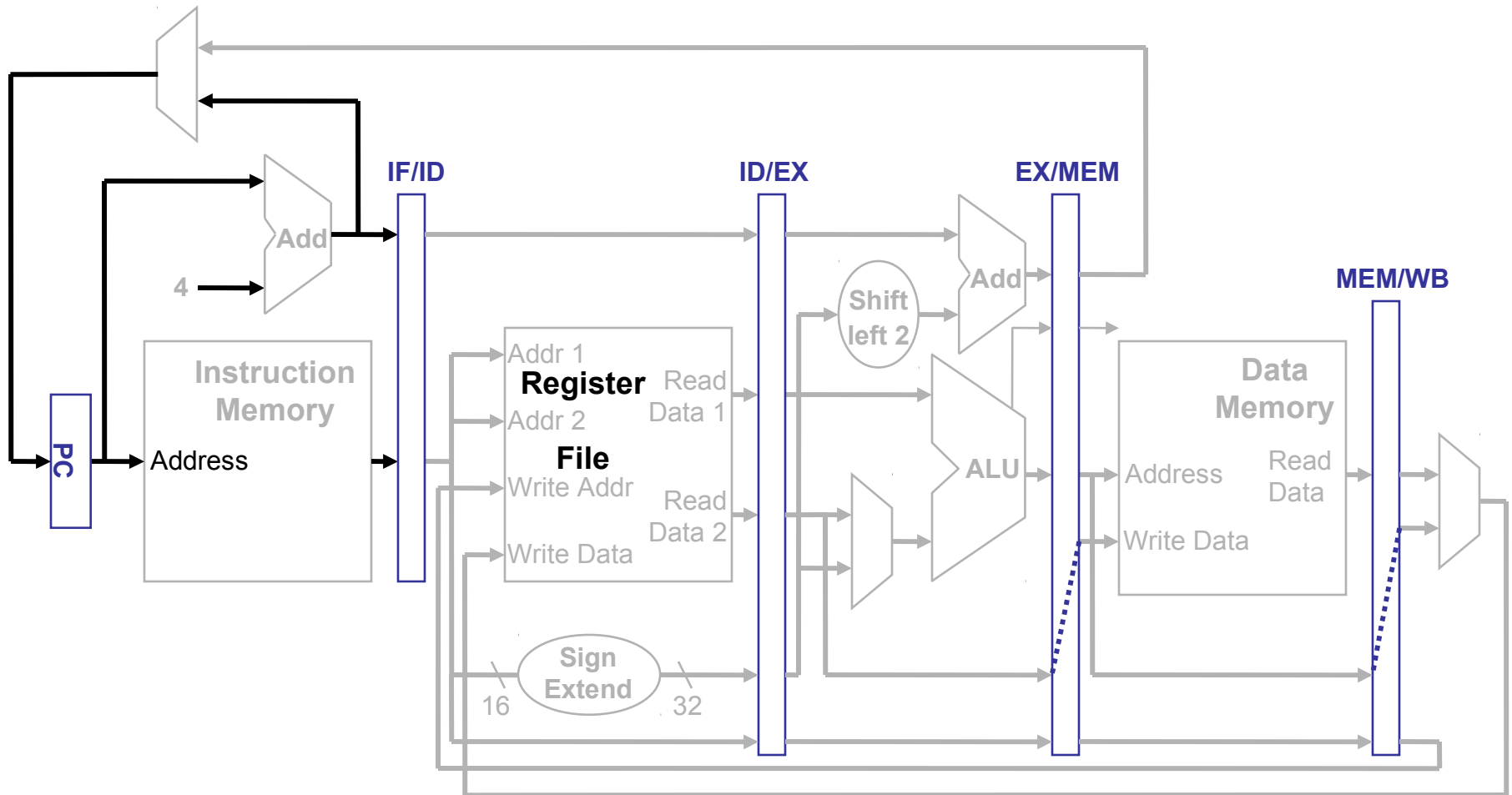
# Load Word Example (Write Back)

- All required values must pass through registers

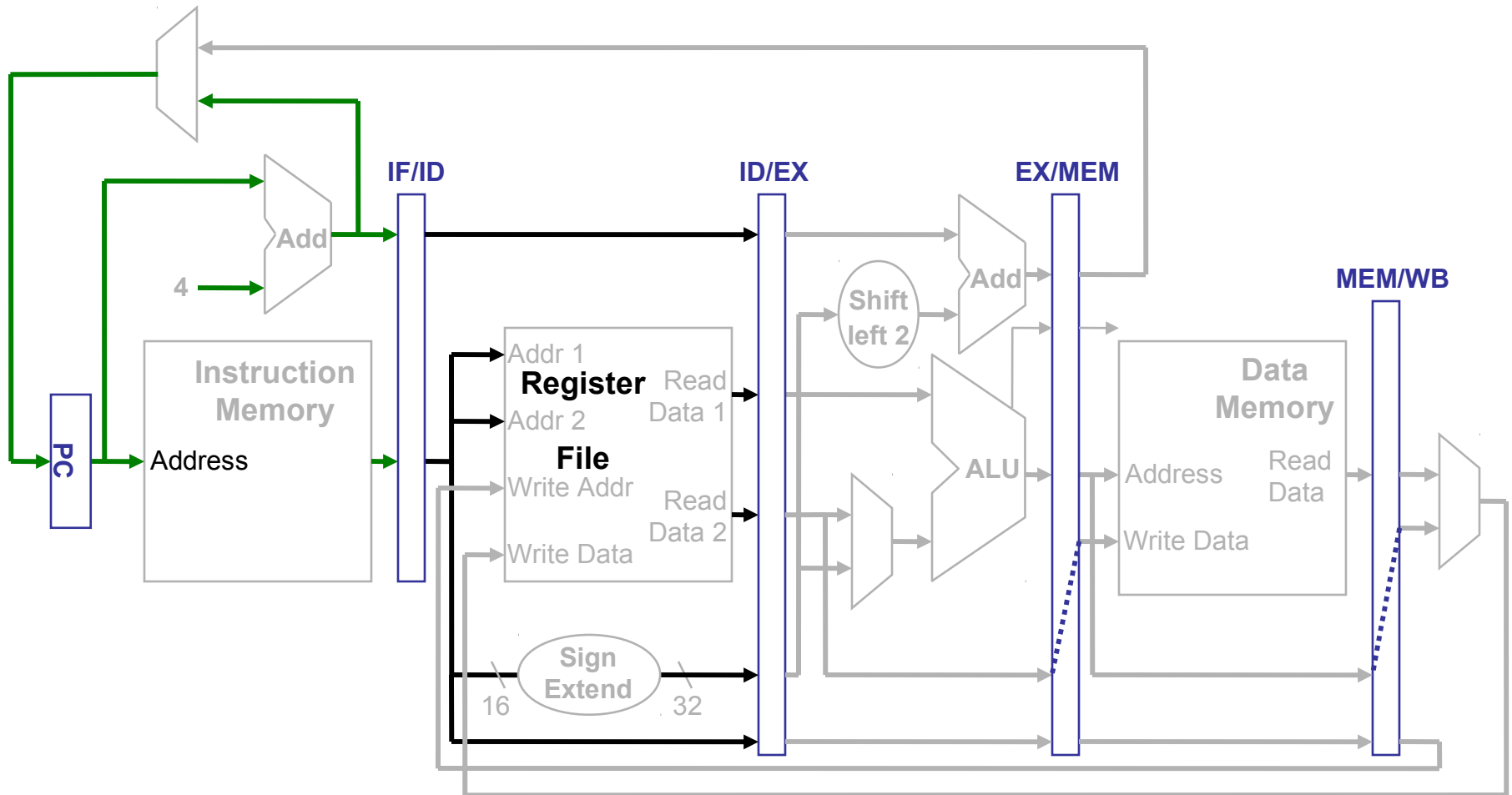




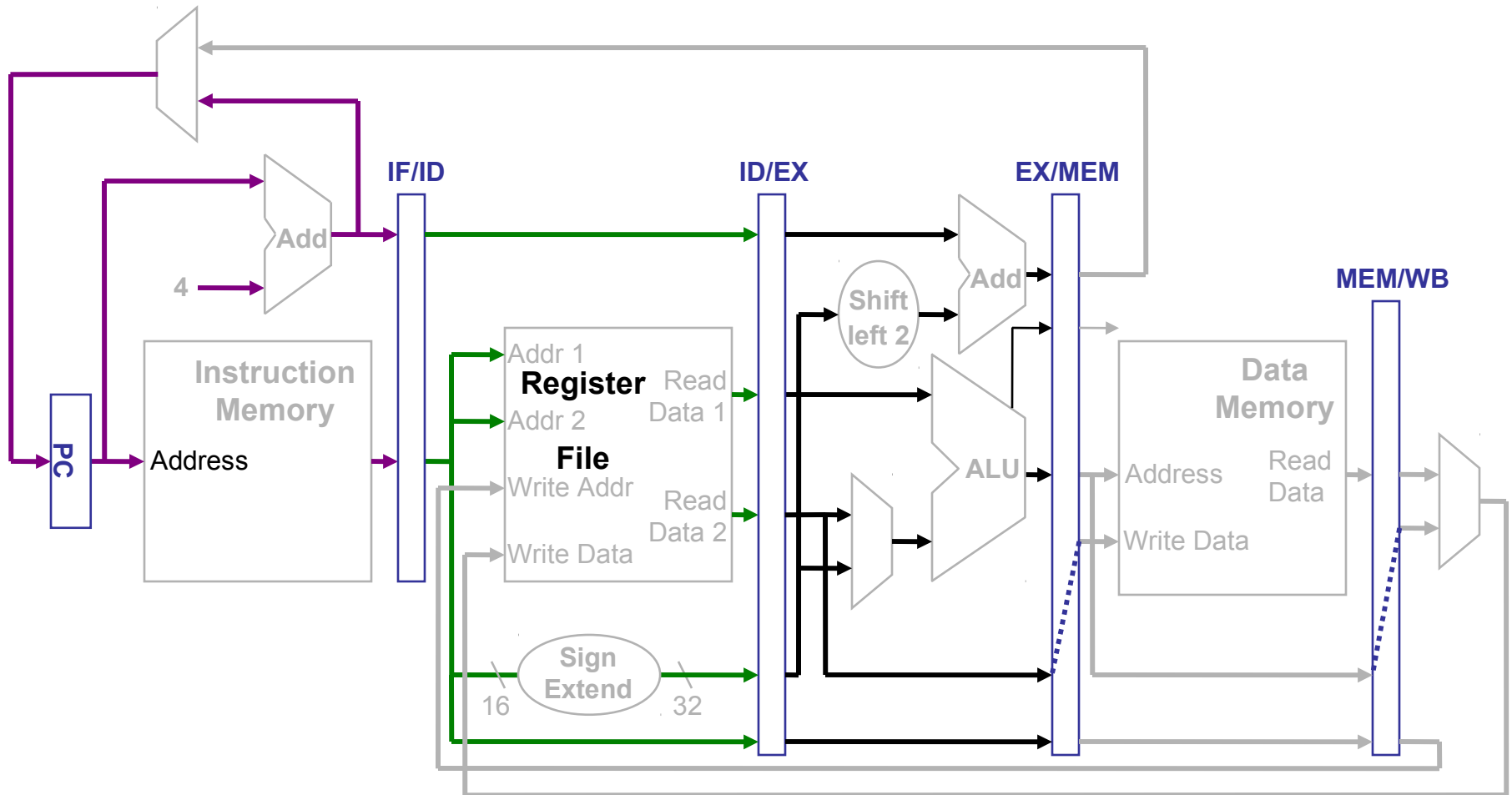
# Load Word Example (Fetch)



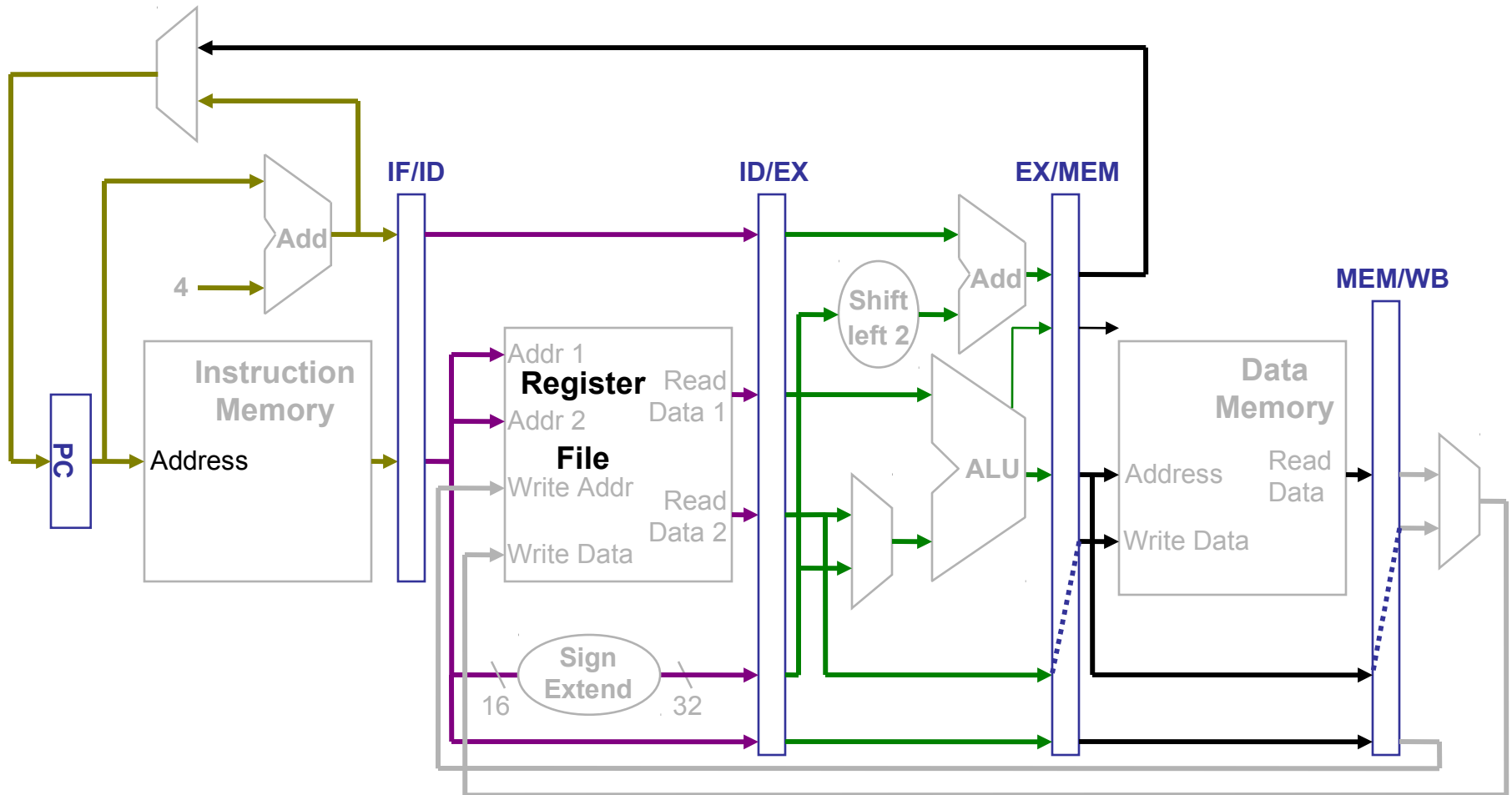
# Load Word Example (Decode)



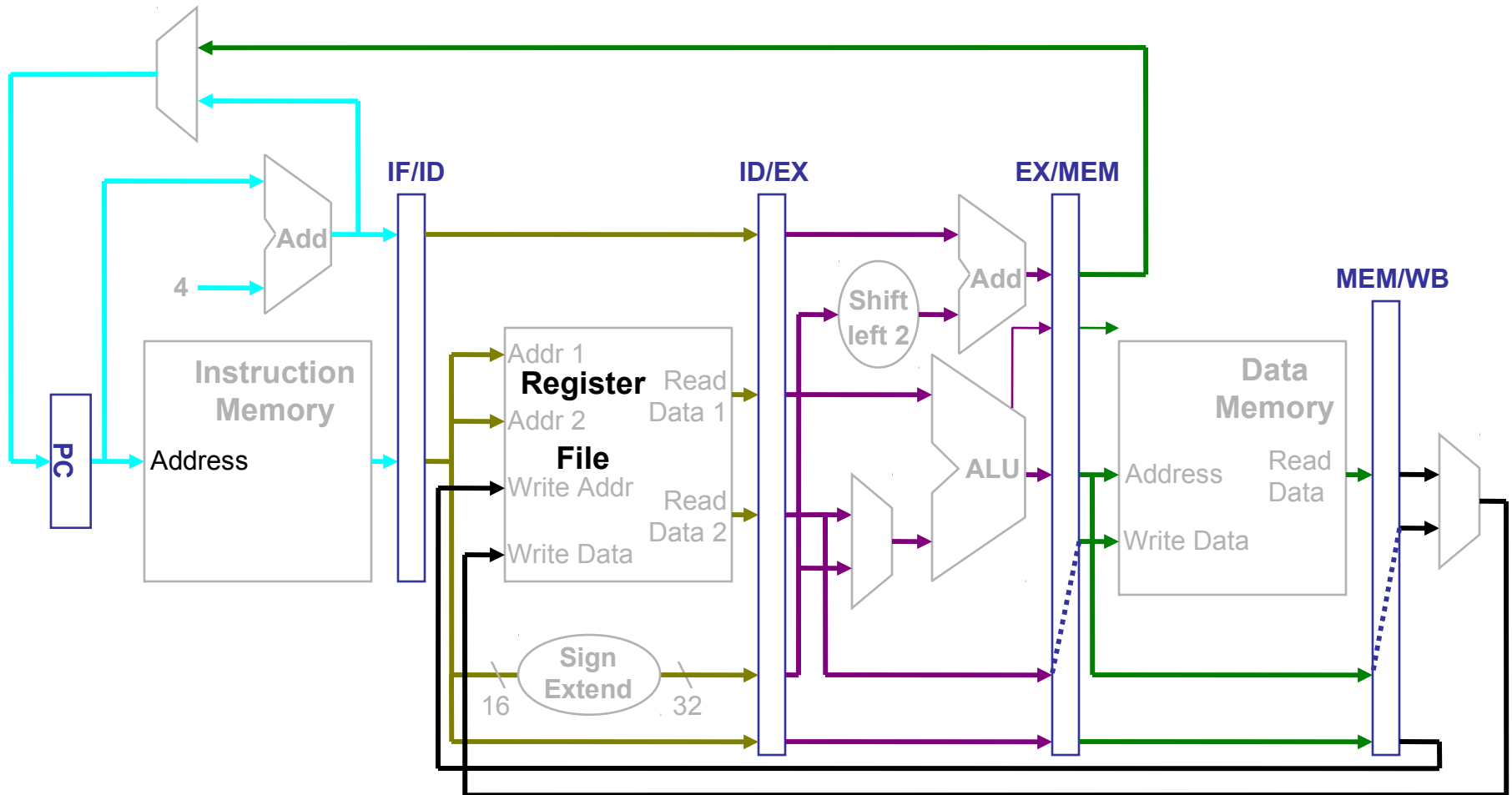
# Load Word Example (Execute)



# Load Word Example (Memory)



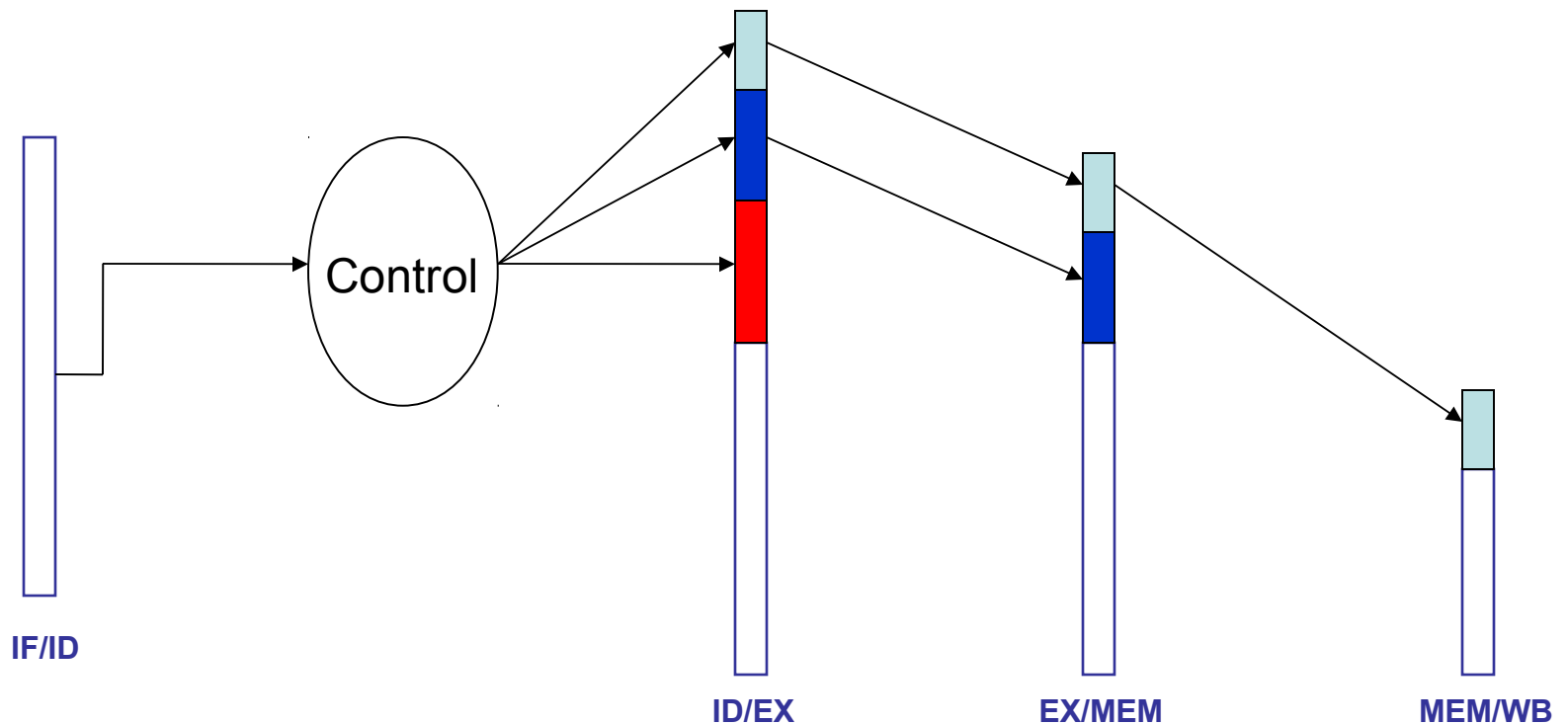
# Load Word Example (Writeback)



# Pipeline Control

---

- Pass control signals using the state registers
  - No need to pass after they are used



# The Pipelined CPU With Control

