1. (2 pts) What concept is at the heart of RISC processing?

2. (2 pts) What are the two main ways to define performance?

3. (3 pts) What is Amdahl's law, in words?

4. (2 pts) What is the only valid and unimpeachable measure of performance?

5. (2 pts) Clock rates have grown by a factor of 1000 while power consumed has only grown by a factor of 30. How was this accomplished?

6. (2 pts) What is the advantage to pipelining a machine? Why not just settle for the single cycle version?

7. (2 pts) What is a "balanced" pipeline?

8. (3 pts) In MIPS, the branch instruction uses the Immediate field to indicate the distance from the current PC that it wants to jump.

   What is that distance measured in?

   How is this accomplished?

   What must be done if you need to jump further than that distance?

9. (6 pts) What are the 4 benchmark types we discussed in class? Do benchmark programs remain valid indefinitely? Why or why not?

10. (3) Why are there multiple dies per silicon wafer? Why not just fabricate one huge die per wafer?

11. (4 pts) Processor A requires 540 instructions to execute a given program, uses 1 cycles per instruction, and has a cycle time of 10 ns. Processor B requires 3 cycle per instruction, but only requires 200 instructions to do the same program. What must the cycle time of Processor B be in order to give the same CPU time as Processor A?

12. (3 pts) Give 3 examples of static branch predictors, in increasing order of accuracy.

13. (3 pts) Give 3 examples of dynamic branch predictors, in increasing order of accuracy.

14. (3 pts) When dealing with control hazards, a prediction is not enough - what else is necessary in order to eliminate stalls?

15. (3 pts) Is it possible to have a WAW dependency in our 5-stage pipeline? Why or why not?

16. (2 pts) We don’t list RAR as being a hazard. Why not?

17. (6 pts) In MIPS, branches and jumps are handled differently. Give 3 ways in which they differ.

18. (6 pts) Our single cycle 8-bit machine is very similar to the MIPS design in the book. List 3 significant differences between the two designs (and obvious, trivial things like "one is 32 bits and one is 8" don't count.)

19. (5 pts) You have an instruction that is a fixed size of 16 bits, and you want to support 32 different operations. You also want to have 16 registers, and use a 3-operand instruction format. If it is possible to this, draw what an instruction would look like. If it is not possible, explain why, and show what you would do to fix the problem.

20. (5 pts) We are going to use microcode to provide the control signals for a multicycle CPU. There are 11 control signals, and the longest instruction takes 5 cycles. In addition, the machine uses a 6-bit opcode. Sketch the simplest microcode configuration that can be used in this machine (how many entries, how wide is each entry, what does each entry contain, etc.)

1. (1) How many entries would it have?

2. (1) How wide would each entry be?

3. (1) What would be contained in each memory location?

4. (2) How would the memory locations be accessed? (In other words, what signals would you use to create the memory address?)

21. (6) The standard MIPS has a 5-stage pipeline, and uses a branch delay slot. If the machine is redesigned to be an 8-stage pipeline, with the following stages:

F D RR E1 E2 M1 M2 WB (where RR stands for Register Read)

How many branch delay slots will this new design require, assuming the branch condition is calculated during E1? During E2?

22. (12 pts) Here is a code sequence.

```
lw      R1, 8(R10)

add     R2, R3, R1

add     R1, R2, R4

sw      R2, 20(R0)

and     R3, R2, R4
```

a) Assuming a standard 5-stage pipeline that does not support hazard detection and does no forwarding, insert as many NOPS as required in order to ensure this code runs correctly. (Remember, writes to the register file occur on the first half of the cycle, and reads occur during the second half).

b) Circle the NOPs that can be removed if forwarding and hazard detection logic is implemented.

c) Reorder the code to remove as many stalls as possible. How many cycles does it take now?

In this question, we are going to wire up a 15-bit processor.

The machine has 3 different instruction formats: R, I, and J.

R-type:

Opcode	rs	rt	rd	funct
14-10	9-8	7-6	5-4	3-0

I-type:

Opcode	rs	rt	Immediate
14-10	9-8	7-6	5-0

J-type:

Opcode	Offset
14-10	9-0

The machine is word-addressable, where a word is 15 bits. Immediates are sign-extended, and in a jump instruction, the jump is not relative to the current PC, but rather is treated as an absolute value.

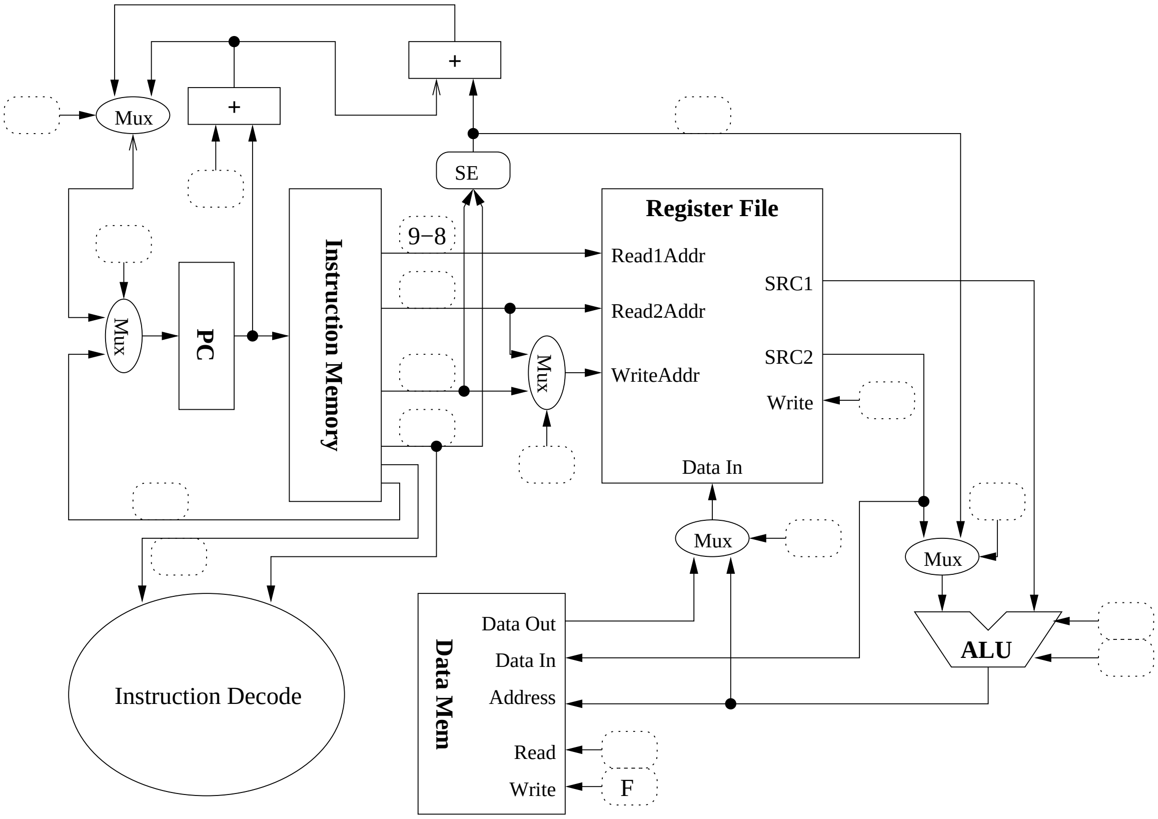
Here are some of the instructions that have been defined:

Name	**Opcode(Funct)**	**Name**	**Opcode(Funct)**	**Name**	**Opcode(Funct)**
lw	00010(xxxx)	sw	00011(xxxx)	NOP	00000(0000)
beqz	00100(xxxx)	j	00101(xxxx)	NOT	01000(0011)
ADD	01000(0000)	ADD Imm	01001(xxxx)	SUB	01000(0100)
AND	01000(0001)	AND Imm	01010(xxxx)	XOR	01000(0101)
OR	01000(0010)	OR Imm	01011(xxxx)	XOR Imm	01100(xxxx)

Here are the 10 control signals.

A) ALU0 C) ALU1 E) ALUSrc G) Br I) MemRead
B) MemWrite D) PCin F) RegWrite H) WrAddr J) WrSrc

19. (8) In the diagram below, make sure all the dashed boxes are filled. Two are already done for you. Use the letters from the previous page instead of the actual names (F instead of RegWrite, for example).



(3) Now, write down the exact boolean equation for the MemRead signal.

20. (4 pts) We need a JAL instruction - let's say it uses register 0. Sketch the changes necessary on the above diagram, and/or describe in words what would need to change in this machine in order to make this work. (Don't forget about instruction set impacts ...)