Very short answer questions. "True" and "False" are considered short answers.

(1) What is the biggest problem facing MIMD processors?

(1) A program's locality behavior is constant over the run of an entire program.

(1) Is it possible to have a WAW hazard in a 7-stage MIPS-like pipeline?

(1) The design of an instruction set has a definite impact on how pipelinable it is.

(1) Give an example of an instruction set that is virtualizable.

(1) Which type of operation is necessary in order to support synchronization?

(1) Which hazard can be eliminated by "throwing more money at the problem"?

(1) Which hazard can be circumvented using "Value prediction"?

(1) Using a different mapping scheme will reduce which type of cache miss?

(1) Which type of cache miss can be reduced by using longer lines?

(1) Which type of cache miss can be reduced by using shorter lines?

(2) What is coherence?

(2) What is consistency?

(2) What is the equation to calculate the average memory access time?

(2) Give two techniques which will help reduce the Hit Time.

(2) Give two techniques will help reduce the Miss Rate.

(2) Give two techniques will help reduce the Miss Penalty.

(2) There are two ways to define performance - what are they?

(2) Predicting a direction is only half of the problem. What else is necessary in order to overcome control flow hazards?

(2) Why is there a "shift left 2" block feeding the PC incrementing adder in MIPS?

(2) What are the two main ways to insert a stall/bubble into the pipeline?

(2) What is a "dirty bit"?

(2) Clock rates have grown by a factor of 1000 while power consumed has only grown by a factor of 30. How was this accomplished?

(2) What is the main difference between a commodity cluster and a custom cluster?

(3) Why is it difficult to come up with good benchmarks for parallel processors?

(3) What is the goal of the memory heirarchy? What two principles make it work?

(2) What is a victim cache, and how does it work?

(2) What is Weak Scaling?

(2) What is a "balanced" pipeline?

(2) What is a TLB, and what does it store?

(3) What are the three types of hazards?

(3) Give 3 different static branch prediction techniques, in order of effectiveness.

(3) Give 3 different dynamic branch prediction techniques, in order of effectiveness.

(3) Assuming a 16-bit address and a 256-byte Direct Mapped cache with a linesize=8, show how an address is partitioned/interpreted by the cache.

(3) Assuming a 16-bit address and a 160-byte 5-way SA cache with a linesize=4, show how an address is partitioned/interpreted by the cache.

(3) Given a 1 Megabyte physical memory, a 24 bit Virtual address, and a page size of 2K bytes, write down the number of entries in the Page Table, and the width of each entry.

(4) Given a 1 Megabyte physical memory, a 32 bit Virtual address, and a page size of 2K bytes, write down the number of entries in the Page Table, and the width of each entry. Is there a problem with this configuration? If so, how can you fix it?

(5) If we are using microprogramming with no optimizations in a machine with a 5-bit opcode, which has 11 control signals and 9 different states, how big is the microprogram ROM (in bits)?

(5) An important program spends 60% of its time doing Floating Point operations, and 40% of its time doing integer arithmetic. By redesigning the hardware you can either make the Floating Point unit take half as long, or the integer unit 90% faster (take 10% as long). Which should you do, and why?

(5) The standard MIPS has a 5-stage pipeline, and uses a branch delay slot. If the machine is redesigned to be an 8-stage pipeline, with the following stages:

F D RR E1 E2 M1 M2 WB (where RR stands for Register Read)

How many branch delay slots will this new design require, assuming the branch condition is calculated during E1? During E2?

(4) What is a dispatch ROM, and where is it used?

(4) Supporting precise interrupts in machines that allow out of order completion is a challenge. Briefly explain why.

(5) What are the 5 registers that had to be added to the single cycle design in order to support multicycle operation in MIPS?

(4) What is the definition of a basic block? Why is there a desire to create a bigger one?

(6) What do the following acronyms stand for?

GPGPU	EPC	IPC
SIMD	UMA	VLIW

(6) Describe the difference between shared memory and message passing machines. Include the impact on design, cost, and programming model.

(6) Understanding the hardware can influence how you write programs. Give 2 examples of how you might write software differently for a heavily pipelined machine verses a non-pipelined one.

(6) In class, we talked about the cycle by cycle steps that occur on different interrupts. For example, here is what happens if there is an illegal operand interrupt generated by instruction i:

	1	2	3	4	5	6	7	8	9	
i	IF	ID	RR	EX	MEM	WB	<- Interrupt detected			
i+1		IF	ID	RR	EX	MEM	WB	<- Instruction Squashed		
i+2			IF	ID	RR	EX	MEM	WB	<- Trap Handler fetched	
i+3				IF	ID	RR	EX	MEM	WB	
i+4					IF	ID	RR	EX	MEM	WB

Fill out the following table if instruction i+1 experiences a fault in the Ex stage (Overflow, for example):

	1	2	3	4	5	6	7	8	9	10	
i	IF	ID	RR	EX	MEM	WB					
i+1		IF	ID	RR	EX	MEM	WB				
i+2			IF	ID	RR	EX	MEM	WB			
i+3				IF	ID	RR	EX	MEM	WB		
i+4					IF	ID	RR	EX	MEM	WB	
i+5						IF	ID	RR	EX	MEM	WB

What happens in this case?

	1	2	3	4	5	6	7	8	9	10	
i	IF	ID	RR	EX	MEM	WB	<- Execution stage has overlflow				
i+1		IF	ID	RR	EX	MEM	WB	<- Inst Read causes Page Fault			
i+2			IF	ID	RR	EX	MEM	WB			
i+3				IF	ID	RR	EX	MEM	WB		
i+4					IF	ID	RR	EX	MEM	WB	
i+5						IF	ID	RR	EX	MEM	WB

(2) What is the maximum number of exceptions that could happen at one time in the above machine?

In this question, we are going to wire up a 24-bit version of the machine used in the midterm.

The machine has 3 different instruction formats: R, I, and J.

R-type:

Opcode	rs	rt	rd
23-18	17-12	11-6	5-0

I-type:

Opcode	rs	rt	Immediate
23-18	17-12	11-6	5-0

J-type:

Opcode	Offset
23-18	17-0

The machine is byte-addressable. Immediates are sign-extended, and jumps are handled similar to what is done in the MIPS processor (they are combined with the PC, although no zero's are appended on the end).

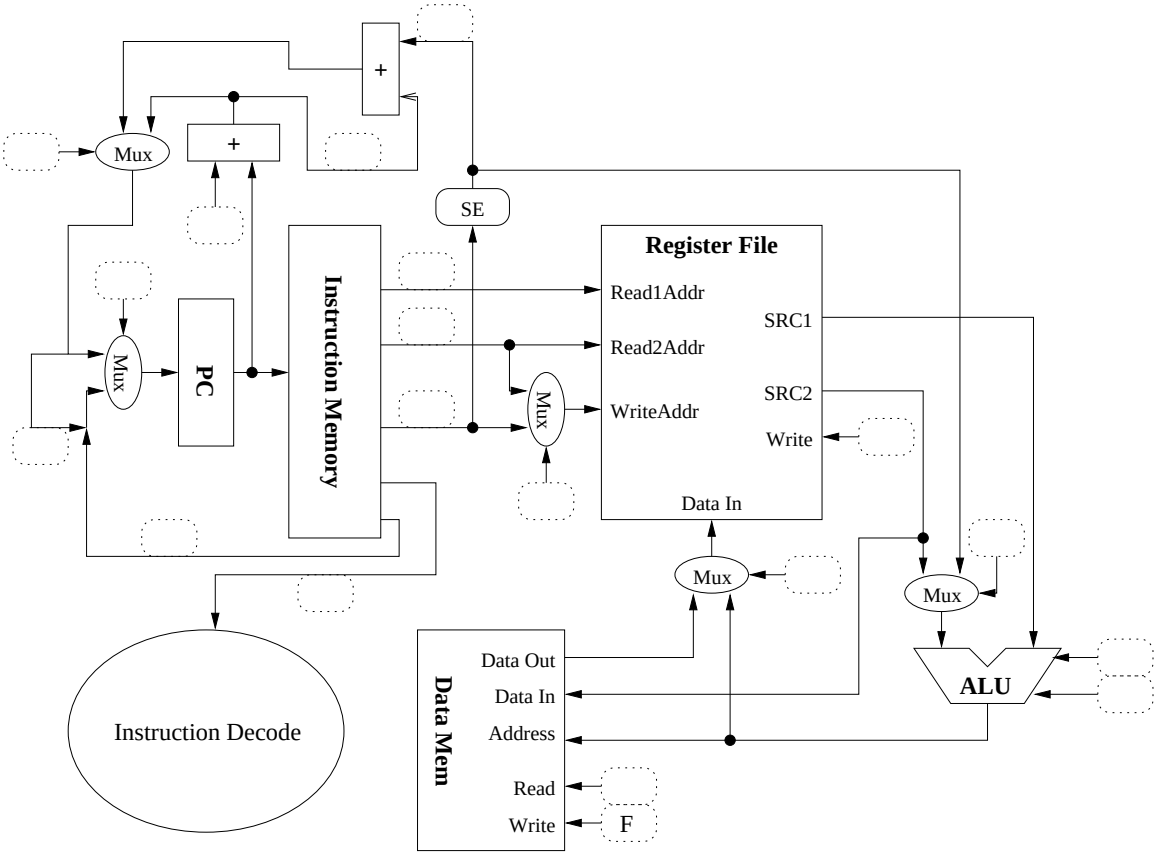
Here are some of the instructions that have been defined:

Name	**Opcode**	**Name**	**Opcode**	**Name**	**Opcode**
lw	0010000	sw	0011000	NOP	0000000
beqz	1000000	j	1100000	NOT	0000001
ADD	0000010	ADD Imm	0000011	SUB	0000100
AND	0000110	AND Imm	0000111	XOR	0001010
OR	0001000	OR Imm	0001001	XOR Imm	0001011

Here are the 10 control signals.

A) PCIn	B) MemRead	C) ALUSource	D) ALU0	E) ALU1
F) MemWrite	G) RegWrite	H) Branch	I) WriteSrc	J) WrAddr

(10) In the diagram below, make sure all the dashed boxes are filled. Two are already done for you. Use the letters from the previous page instead of the actual names (F instead of MemWrite, for example).



(3) Now, write down the exact boolean equation for the Branch signal.

(6) We need a JAL instruction - let's say it uses register 12. Sketch the changes necessary on the above diagram. In addition, briefly describe in words what would need to change in this machine in order to make this work. (Don't forget about instruction set impacts ...)