The first 5 Questions are very short answer questions:

1. (1pts) What is the Hamming distance between these two bit patterns: 0011 and 0100?

2. (3pts) How far apart must valid code words be to allow Single Error Detection (SED)?
   Double Error Correction (DEC)?
   Quadruple (4) Error Correction Quintuple (5) Error Detection (QECQED)?

3. (3pts) What is the difference between the Mealy and Moore models of sequential design?

4. (3pts) What is the difference between a Flip-flop and a Latch?

5. (3pts) Write the equation for the carry into the 5th adder cell in an ALU using carry-lookahead, in terms of P's and G's.

6. (2pts) Write next to each of the following equations if they are SOP or POS.

   $\overline{(\overline{X}+Y+\overline{Z})}(X+Y+\overline{Z})$

   $\overline{X}Y\overline{Z}+XY\overline{Z}$

7. (3pts) Show how to make an OR, an AND, and a NOT gate using using only NAND gates.

8. (3pts) Show how to make an SR latch using only NAND gates.

9. (10 pts) Assume you have 12-bit data words, and your memory system supports Single Error Correction. For each of the following patterns recieved from memory identify and correct any errors that may have occurred during transmission or storage. Assume the same organization of carry and data bits as we used in class. The first one is done for you.

   Given: **0 0 1 0 1 0 1 1 0 0 1 0 1 0 1 1 0** The Data Word is: **010101101011**

   Given: **1 1 0 1 1 0 1 1 1 0 0 1 1 0 0 1 0** The Data Word is:

10. (9 pts) You have derived the following karnaugh maps for the inputs to a JK flip-flop. Unfortunately, the parts department just called and your company is completely out of JK flip-flops. All they have left in stock is Toggle flip-flops, which you will have to use instead. Show the resulting karnaugh map for the modified version of the circuit (the one that uses the Toggle instead of the JK flip-flop.)

J

Y2 \ Y1X	00	01	11	10
0	1	d	d	1
1	1	d	d	1
3		d	d	
2		d	d	

Y3

K

Y2 \ Y1X	00	01	11	10
0	d	1	1	d
1	d			d
3	d	1	1	d
2	d	1	1	d

Y3

11. (20pts) Given the following state transition table, draw the Karnaugh maps for Y1', Y2', and Y3', and Z in terms of X, Y1, Y2 and Y3, and then write minimum boolean equations for each. Use Don't Care variables if they are available.

Present State			Next State						Output (Z)	
			X=0			X=1			X=0	X=1
Y1	Y2	Y3	Y1'	Y2'	Y3'	Y1'	Y2'	Y3'		
0	0	0	1	0	0	1	0	1	0	1
0	0	1	1	0	1	1	1	1	0	0
0	1	1	1	0	0	1	1	0	0	0
1	0	0	0	0	1	0	0	0	1	1
1	0	1	1	0	1	0	1	1	0	1
1	1	0	0	0	1	0	0	0	1	1
1	1	1	1	0	1	1	1	0	0	0

12. (20 pts) Given the following Karnaugh maps, implement the sequential machine using a JK FF for Y1, a Toggle FF for Y2, and an SR FF for Y3. You do not need to draw the gates, but you do need to write down the input equations for each of the inputs of each of the Flip Flops in the circuit.

Y1'

Y2 \ Y3X	00	01	11	10
00	1			1
01	1	1	1	1
11		1	1	
10				

Y1

Y2'

Y2 \ Y3X	00	01	11	10
00	1	1	1	1
01		d	1	
11		1	1	
10	1			1

Y1

Y3'

Y2 \ Y3X	00	01	11	10
00	1	1		
01		1	1	
11		1	1	
10			1	1

Y1

13. (20 pts) You have been hired by the country of Freedonia to design a toll both for their national highway. In Freedonia there are only two types of coins, the 50 Somolian piece and the 30 Somolian piece. The toll booth requires an input of at least 115 Somolians before the toll gate is raised, and gives no change. Only one coin can be deposited at a time. Let X1=50 Somolians and X2=30 Somolains. Z=1 indicates the Gate should be raised, Z=0 signals No Go Joe. (Everyone in Freedonia is named "Joe".)

Draw the State Transistion Diagram (the circles and the arcs) for this finite state machine. Let S0=nothing deposited (the Start state). Once you have a state transition diagram, assign bit patterns to each state and write down the corresponding state transition table. Assume you are using a Mealy model. Also, label the transitions on the diagram using the following format:

$$\frac{X1\,X2}{Z}$$

So, for example,

$$\frac{0\;1}{0}$$

would be used to indicate that a 30 Somolian piece was deposited, and the output at that point should be a 0.