1. (2pts) Write the equation for the carry out of the 5th adder cell in an ALU using carry-lookahead, in terms of P's and G's.

2. (2 pts) What is a Karnaugh Map?

3. (2pts) What is the difference between a Flip-Flop and a latch?

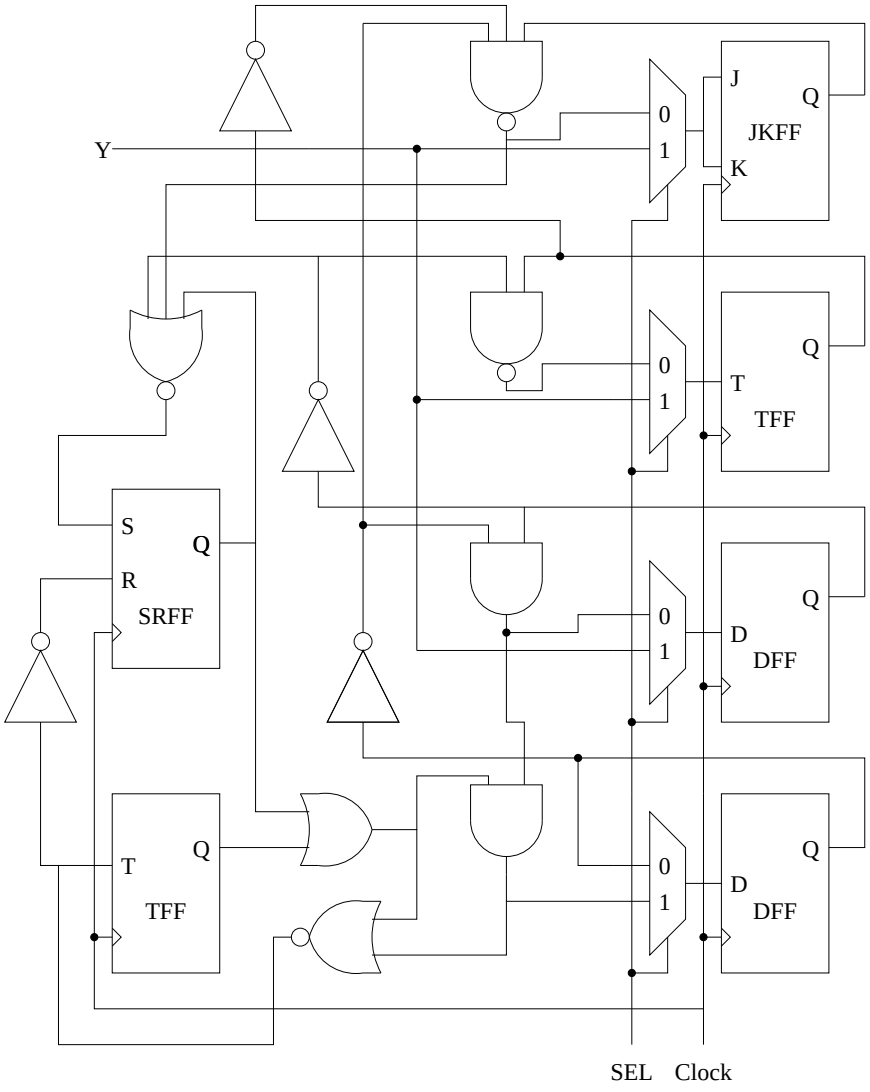
4. (3pts) What is the difference between the Mealy and Moore models of sequential design? What is the advantage to the Moore approach?

5. (4pts) Using a 4-1 mux, implement the following function:
   (Cbar) + (Abar * B * Cbar)

6. (12 pts) Assuming rising edge-triggered flipflops, what is the maximum clock frequency possible for the following circuit? (In other words, what is the maximum clock frequency that will still guarantee correct behavior?) Use the following delay values, and assume all input signals become valid at time 0. (Tprop is the propagation time for the flipflop, the time it takes from the rising edge of the clock until the output of the FF is valid.)

AND: 4ns OR: 5ns NAND: 3ns NOR: 4ns NOT: 1ns MUX: 5ns
Tprop (TFF): 10ns Tsetup (TFF): 4ns Thold (TFF): 1ns
Tprop (DFF): 7ns Tsetup (DFF): 3ns Thold (DFF): 1ns
Tprop (JKFF): 8ns Tsetup (JKFF): 4ns Thold (JKFF): 1ns
Tprop (SRFF): 11ns Tsetup (SRFF): 4ns Thold (SRFF): 1ns

Note: You must show the path in order to get credit.



7. (2pts) How far apart must valid code words be to allow Quadruple (4) Error Detection (QED)?
Sextuple (6) Error Correction (SEC)?

8. (6 pts) Here is a 12-bit Error Correction code format (same one used in class):

$$d_8 \;\; d_7 \;\; d_6 \;\; d_5 \;\; C_4 \;\; d_4 \;\; d_3 \;\; d_2 \;\; C_3 \;\; d_1 \;\; C_2 \;\; C_1$$

a. Given the *data* bit pattern

1 0 0 1 1 1 0 0

in a machine using the above ECC code, what bit pattern gets sent to memory? (No credit will be given without work being shown.)

9. (6pts) In the same machine as above, the following bit pattern is retrieved from memory:

0 1 0 1 1 0 1 0 1 1 1 0

Assuming the above Error Correction code format, identify and correct any errors that may have occurred during transmission or storage. (No credit will be given without work being shown.)

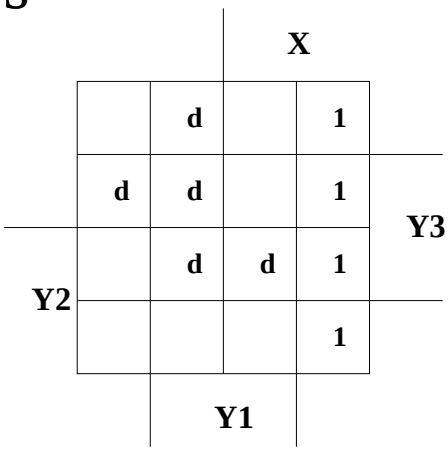
10. (10 pts) You have been asked to create a new flipflop, which has two inputs - the "B" and the "U". All you have to work with is a JKFF. The BUFF is to exhibit the following behavior:

Present State		Next State
B	U	Z’
0	0	1
0	1	0
1	0	Zbar
1	1	Z

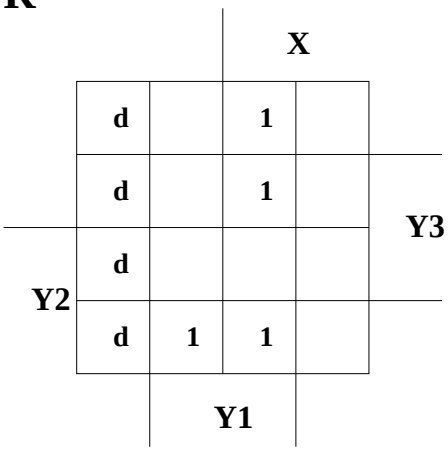
Write down what the T input must be (in terms of B, U, and Z) in order to provide the desired functionality. Be sure to minimize the equations.

10. (6 pts) You have derived the following karnaugh maps for the inputs to a SR flip-flop. Unfortunately, the parts department just called and your company is completely out of SR flip-flops. All they have left in stock is T flip-flops, which you will have to use instead. Show the resulting karnaugh map for the modified version of the circuit (the one that uses the T instead of the SR flip-flop.) You do **not** have to write down the minimized equation.

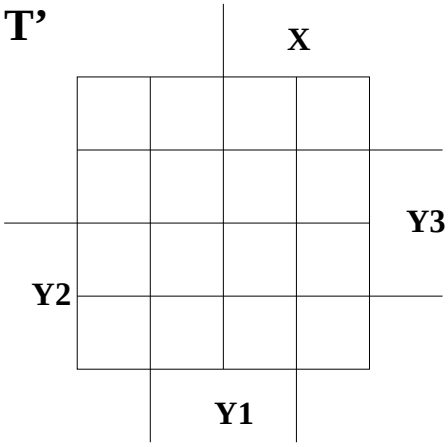
S'



R'

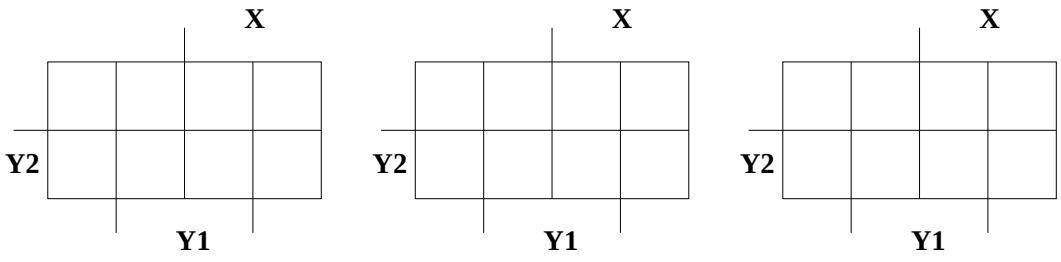


T'



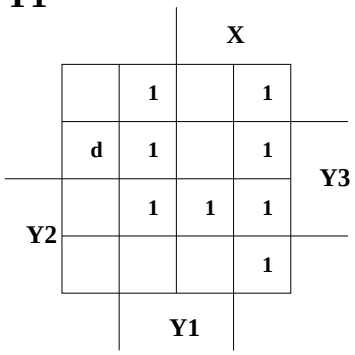
11. (12) Given the following table, draw the Karnaugh maps for Y1', Y2' and Z in terms of X, Y1 and Y2, and then write **minimum** boolean equations for each.

Present State (Y1 Y2)	Next State X=0 (Y1' Y2')	Next State X=1 (Y1' Y2')	Output X=0	Output X=1
01	01	10	0	0
10	01	11	0	1
11	01	01	1	1

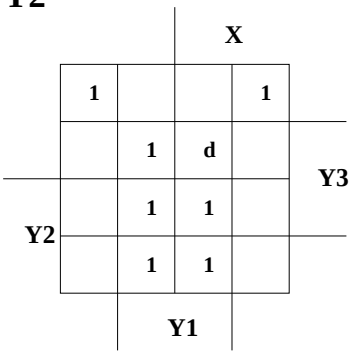


12. (15 pts) Given the following Karnaugh maps, implement the sequential machine using an SR FF for Y1, a JK FF for Y2, and a T FF for Y3. You do not need to draw the gates, but you do need to write down the **minimized** input equations for each of the inputs of each of the Flip Flops in the circuit.

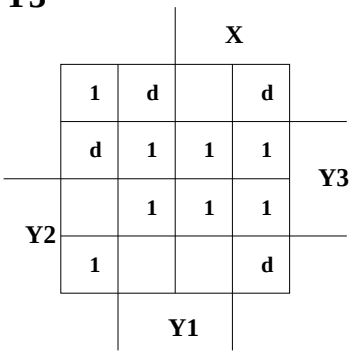
Y1'

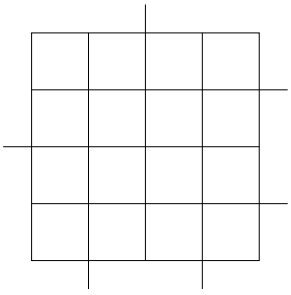


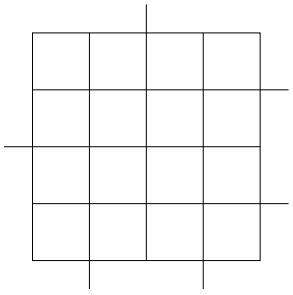
Y2'

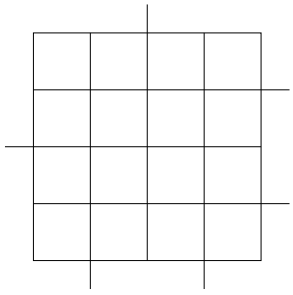


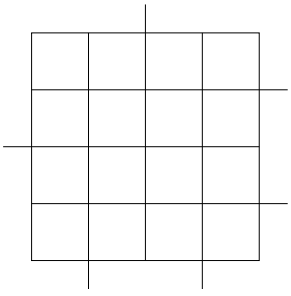
Y3'

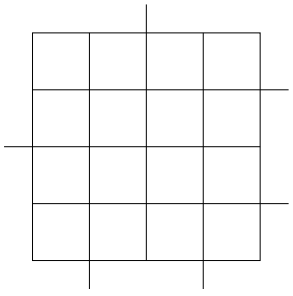


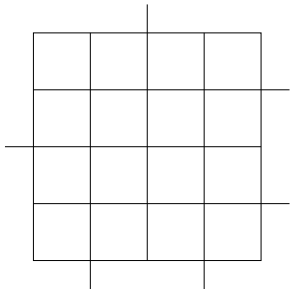












13. (10 pts) There's a machine, it's coin-operated, it does something, blah blah blah. Two kinds of coins, X1 (worth 2) and X2 (worth 1), can't put both in simultaneously. Machine requires sum of 3 in order to do its thing. The machine must give change.

    Using a Mealy model, draw the State Transistion Diagram (the circles and the arcs) for this finite state machine. Label the transitions on the diagram using the format we used in class (inputs over outputs). Let state S0=no money input (the Start state).

    (6) Now, repeat the same problem using a Moore model.

14. (8 pts) Using this state transition diagram, minimize the number of states necessary and then assign bit patterns to each state. (Make a state transition table, in other words.)