1. (1pts) What is the Hamming distance between these two bit patterns: 0011 and 1101?

2. (2pts) Write the equation for the carry out of the 3rd adder cell in an ALU using carry-lookahead, in terms of P's and G's.

3. (2 pts) What is a Karnaugh Map?

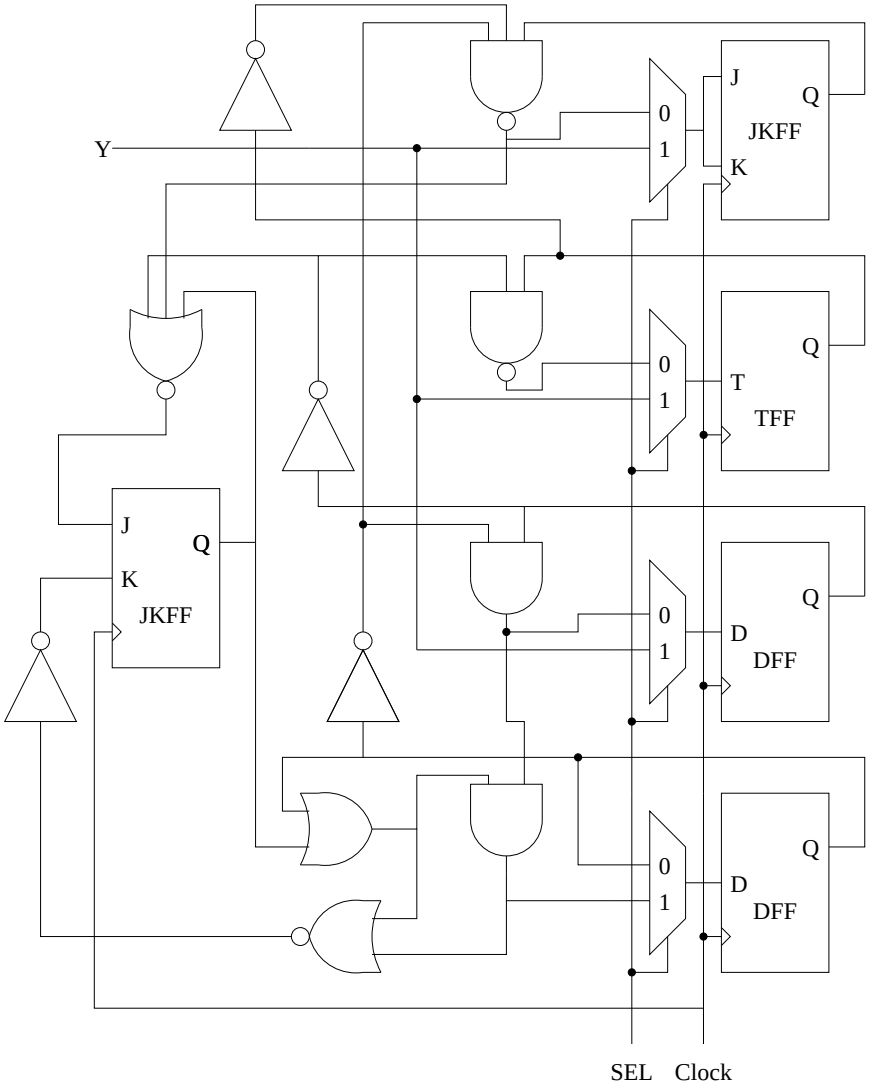
4. (2pts) What is the difference between a Flip-Flop and a latch?

5. (3pts) What is the difference between the Mealy and Moore models of sequential design? What is the advantage to the Moore approach?

6. (3pts) Using only basic gates (AND, OR, NOT, NAND, etc.) draw a flip flop.

7. (12 pts) Assuming edge-triggered flipflops, what is the maximum clock frequency possible for the following circuit that will still guarantee correct behavior? Use the following delay values, and assume all input signals become valid at time 0 (including Y). **You must show the worst case path in order to receive full credit.**

AND: 3ns NAND: 4ns OR: 3ns NOR: 2ns NOT: 1ns MUX: 5ns
Tprop (DFF): 7ns Tsetup (DFF): 5ns Thold (DFF): 3ns
Tprop (TFF): 8ns Tsetup (TFF): 3ns Thold (TFF): 2ns
Tprop (JKFF): 8ns Tsetup (JKFF): 2ns Thold (JKFF): 2ns



8. (3pts) How far apart must valid code words be to allow Triple (3) Error Detection (TED)?
Quadruple (4) Error Correction (QEC)?
Quintuple (5) Error Correction Sextuple (6) Error Detection (QECSED)?

9. (6 pts) Here is a 12-bit Error Correction code format (same one used in class):

$$d_8 \;\; d_7 \;\; d_6 \;\; d_5 \;\; C_4 \;\; d_4 \;\; d_3 \;\; d_2 \;\; C_3 \;\; d_1 \;\; C_2 \;\; C_1$$

a. Given the *data* bit pattern

0 0 1 0 1 1 0 1

in a machine using the above ECC code, what bit pattern gets sent to memory? (No credit will be given without work being shown.)

10. (6pts) In the same machine as above, the following bit pattern is retrieved from memory:

0 1 1 0 0 1 1 0 0 1 1 0

Assuming the above Error Correction code format, identify and correct any errors that may have occurred during transmission or storage. (No credit will be given without work being shown.)

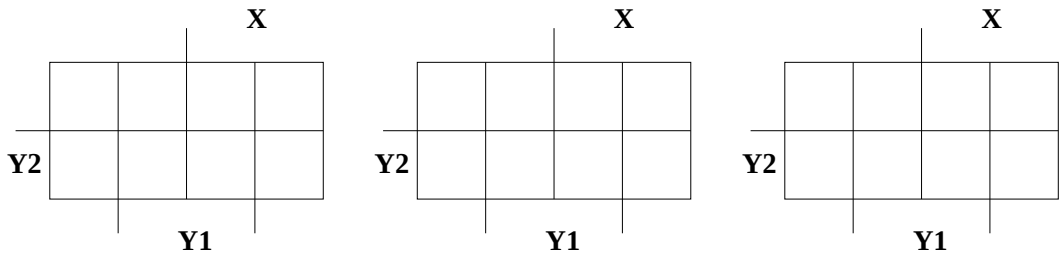
11. (11 pts) You have been asked to create a new flipflop, which has two inputs - the "TE" and the "ST". All you have to work with is a TFF. The TESTFF is to exhibit the following behavior:

Present State		Next State
TE	ST	Z’
0	0	1
0	1	Zbar
1	0	0
1	1	Z

Write down what the T input must be (in terms of TE, ST, and Z) in order to provide the desired functionality. Be sure to minimize the equations.

12. (12) Given the following table, draw the Karnaugh maps for Y1', Y2' and Z in terms of X, Y1 and Y2, and then write **minimum** boolean equations for each.

Present State (Y1 Y2)	Next State X=0 (Y1' Y2')	Next State X=1 (Y1' Y2')	Output X=0	Output X=1
00	11	01	0	0
01	11	11	0	0
11	00	01	1	1



13. (15 pts) Given the following Karnaugh maps, implement the sequential machine using an SR FF for Y1, a JK FF for Y2, and a T FF for Y3. You do not need to draw the gates, but you do need to write down the **minimized** input equations for each of the inputs of each of the Flip Flops in the circuit.

Y1'

Y2 \ Y3X	00	01	11	10
00	1	1		d
01	d	1		1
11		1		
10		1		d

Y2'

Y2 \ Y3X	00	01	11	10
00	1	1	d	1
01				
11	1	1	1	
10		1	1	

Y3'

Y2 \ Y3X	00	01	11	10
00				d
01	1	1	1	1
11	1			1
10		1	1	d

14. (8 pts) The Others have built some sort of coin-operated machine. OtherLand has two coins: the Alpha (worth 10 units) and the Beta (worth 15). This machine does something if a total of 45 units has been inserted. Let X1 be the Alpha and X2 the Beta, and assume both coins cannot be inserted simultaneously (Thus 10 = Alpha inserted, 01 = a Beta.) The machine must give change.

    Using a Mealy model, draw the State Transistion Diagram (the circles and the arcs) for this finite state machine. Label the transitions on the diagram using the format we used in class (inputs over outputs). Let state S0=no money input (the Start state).

    (6) Now, repeat the same problem using a Moore model.

15. (8 pts) Using this state transition diagram, minimize the number of states necessary and then assign bit patterns to each state. (Make a state transition table, in other words.)