Given a 32-byte Direct Mapped Cache with a line size of 2 words, a word size of 16 bits, a 128-byte memory containing the values shown, and the following address reference sequence for a byte-addressable machine:

0x0E,0x1A,0x0C,0x26,0x06

Fill in the Cache's Tag and Data values after each memory reference has been processed. Assume all the entries in the tag array are initially invalid.

Memory Contents at Address **XY**																
Most Significant Digit(**X**)	Least Significant Digit (**Y**)															
	0	1	2	3	4	5	6	7	8	9	a	b	c	d	e	f
0	23	20	6d	61	74	74	27	73	20	67	76	69	65	77	20	73
1	68	65	6c	6c	20	73	63	72	69	70	74	0a	73	65	74	20
2	67	66	69	6c	65	20	3d	20	24	31	0a	09	65	63	68	6f
3	20	2d	6e	20	22	67	67	72	61	70	68	20	24	67	66	69
4	6c	65	2e	2e	2e	22	20	0a	09	65	63	68	6f	20	22	2e
5	73	70	20	32	22	20	3e	21	20	2f	74	6d	70	2f	74	65
6	6d	70	24	24	2e	6e	72	0a	09	65	63	68	6f	20	22	2e
7	70	6f	20	2b	30	2e	35	69	22	20	3e	3e	20	2f	74	6d

Tag Array	Contents of Tag Array after processing address (Time ->)				
Address	0E	1A	0C	26	06
0					
1					
2					
3					
4					
5					
6					
7					

Data Array	Contents of Data Array after processing address (Time ->)				
Address	0E	1A	0C	26	06
0					
1					
2					
3					
4					
5					
6					
7					

Given a 32-byte 2-way Set Associative Cache with a line size of 2 words, a word size of 16 bits, a 128-byte memory containing the values shown, and the following address reference sequence for a byte-addressable machine:

0x0E,0x36,0x1A,0x0C,0x26,0x06

Use an LRU replacement scheme.

Memory Contents at Address **XY**																
Most Significant Digit(**X**)	Least Significant Digit (**Y**)															
	0	1	2	3	4	5	6	7	8	9	a	b	c	d	e	f
0	23	20	6d	61	74	74	27	73	20	67	76	69	65	77	20	73
1	68	65	6c	6c	20	73	63	72	69	70	74	0a	73	65	74	20
2	67	66	69	6c	65	20	3d	20	24	31	0a	09	65	63	68	6f
3	20	2d	6e	20	22	67	67	72	61	70	68	20	24	67	66	69
4	6c	65	2e	2e	2e	22	20	0a	09	65	63	68	6f	20	22	2e
5	73	70	20	32	22	20	3e	21	20	2f	74	6d	70	2f	74	65
6	6d	70	24	24	2e	6e	72	0a	09	65	63	68	6f	20	22	2e
7	70	6f	20	2b	30	2e	35	69	22	20	3e	3e	20	2f	74	6d

Tag Array		Contents of Tag Array after processing address (Time ->)					
Set	Address	0E	36	1A	0C	26	06
0	0						
	1						
1	2						
	3						
2	4						
	5						
3	6						
	7						

Data Array	Contents of Data Array after processing address (Time ->)					
Address	0E	36	1A	0C	26	06
0						
1						
2						
3						
4						
5						
6						
7						

The following tables contain information about a segmented, paged virtual memory system and certain select memory locations. Total physical memory size is 2K bytes. All numbers in this table are in Hex unless otherwise noted.

Segment Table		
Entry Number	Presence Bit	Page Table
0	1	1
1	0	0

Page Table 0			
Entry Number	Presence Bit	Disk Address	Physical Page Number
0	1	1234123	0x0
1	0	0893748	0x3
2	1	2489567	0x1
3	1	9623873	0x2

Page Table 1			
Entry Number	Presence Bit	Disk Address	Physical Page Number
0	1	1234123	0x1
1	0	0893748	0x0
2	1	2489567	0x3
3	1	9623873	0x2

Memory	
Address	Contents
0x03A4	0x7230
0x05A4	0x86a9
0x06A4	0x9723
0x07A4	0x3423
0x0AA4	0x8876
0x0FA4	0x2373
0x11A4	0x1346
0x17A4	0x6792
0x1EA4	0x5292
0x37A4	0x7974
0x3BA4	0x3205
0x67A4	0x6623

Assuming 512-byte pages, convert the virtual address **0x7A4** into a physical address.
(**0x7A4** is **0 1 1 1 1 0 1 0 0 1 0 0** in binary).

What is the value in memory stored at the physical address corresponding to the virtual address **0x7A4**?