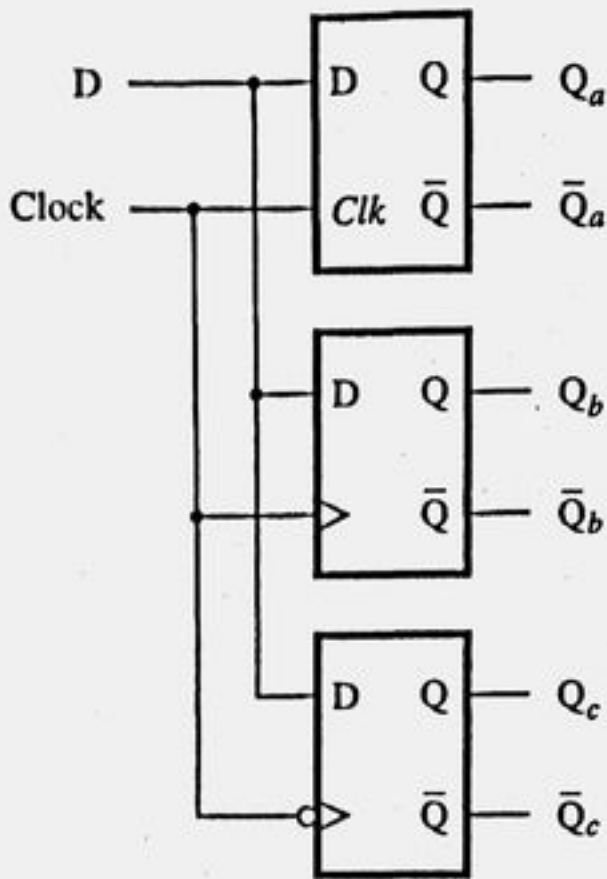
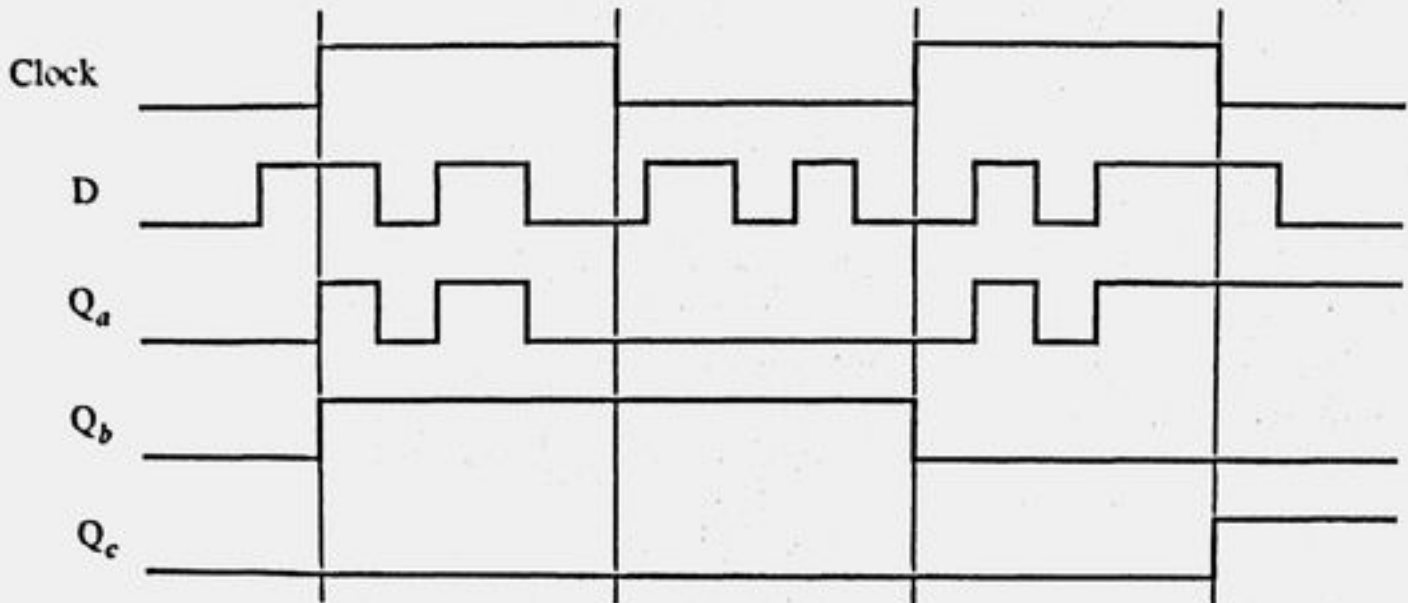


7.4 MASTER-SLAVE AND EDGE-TRIGGERED D FLIP-FLOPS



(a) Circuit



(b) Timing diagram

Figure 7.12 Comparison of level-sensitive and edge-triggered D storage elements.