Partial Resolution in Branch Target Buffers

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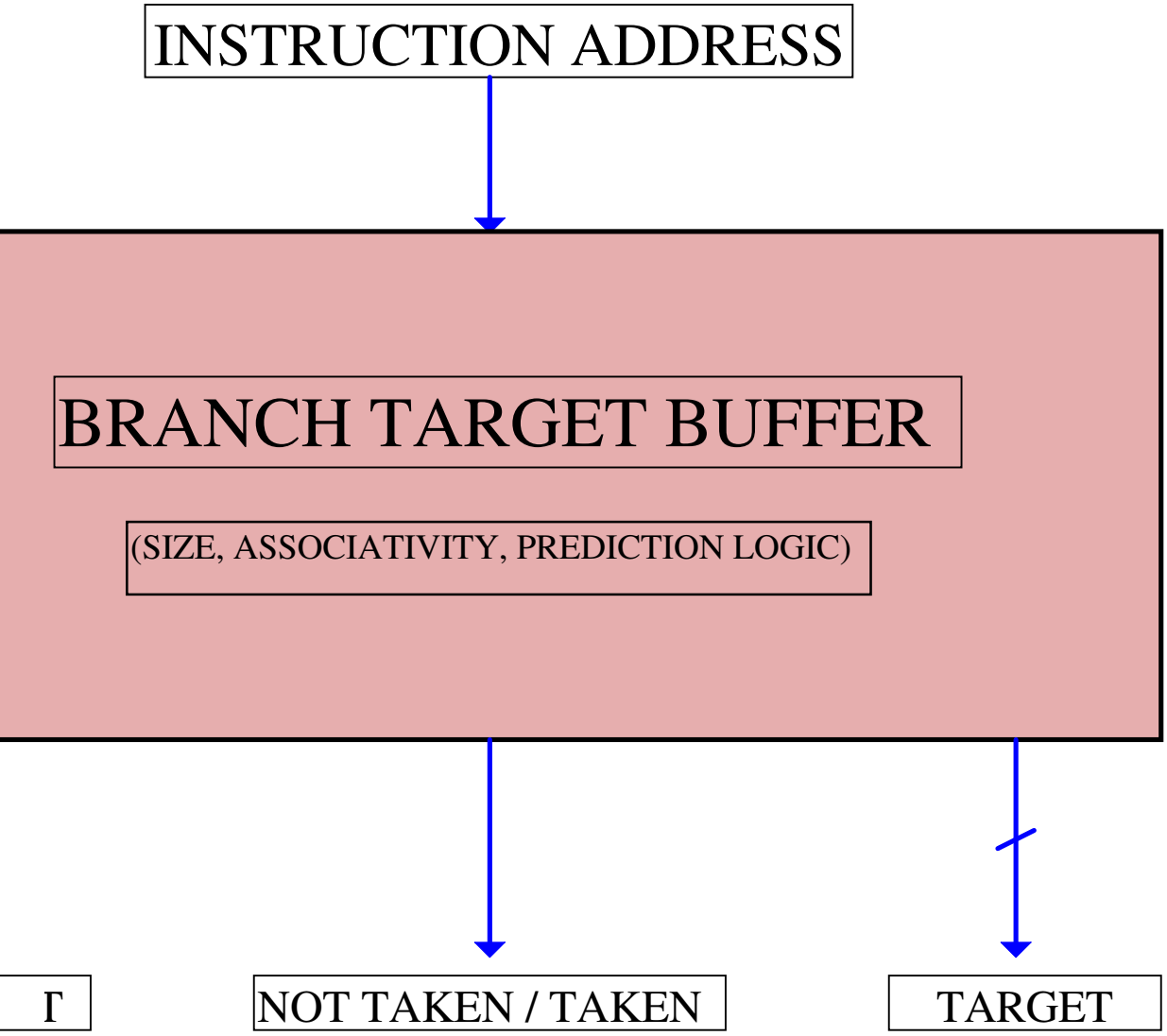
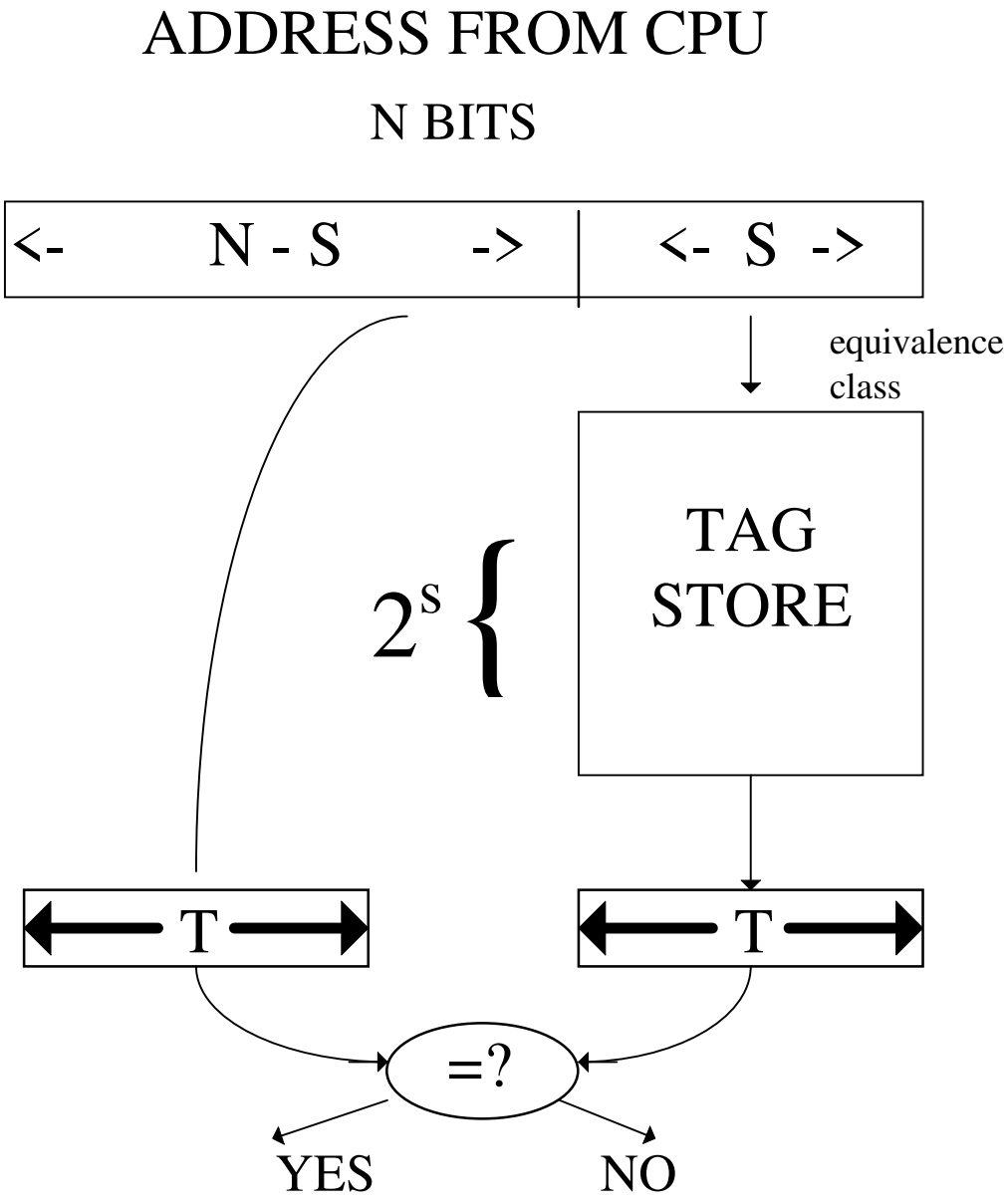
t buffers, or BTBs, function as a cache
f recently accessed program branches.

e caches.

es, correct output is not essential for pr
an make cost/performance tradeoffs by
width of the tag store.

ate large reductions in tag store possi
formance costs.


INSTRUCTION ADDRESS
BRANCH TARGET BUFFER
(SIZE, ASSOCIATIVITY, PREDICTION LOGIC)
Γ
NOT TAKEN / TAKEN
TARGET



olution	present	not present
resolution	*may be present*	not present

“ ıot taken” / taken
ıon-branch instruction
ection is “not taken” / taken
lress from BTB is not correct / is correct
spond to misprediction penalties

Comments
ken” branch miss
ranch miss, penalty
nch miss
sible -- non-branch instructions never taken
sible -- all misses are predicted “not taken”
ken” branch hit
ranch hit, incorrect prediction, penalty
nch instruction aliased to branch, predicted not taken. No penalty.
sible -- non-branch instructions never taken
ken” branch hit, incorrect prediction, penalty
ranch hit, correct prediction but bad target, penalty
ranch hit, correct prediction.
ınch instruction aliased to branch, predicted taken, penalty
nch instruction aliased to branch, predicted taken but target matches address inst. No penalty.
sible -- non-branch instructions never taken

A taxonomy of BTB access types

The SPEC Integer Benchmarks
(simulated to completion)

ıchmark	input file(s)	# instructions
ıpress	in	94,915,891
resso	bca.in	511,627,275
tott	int_pri_3.eqn	1,025,792,632
	*.i	45,099,325
	loada1	926,383,440
p	li-input.lsp	5,821,639,146

n

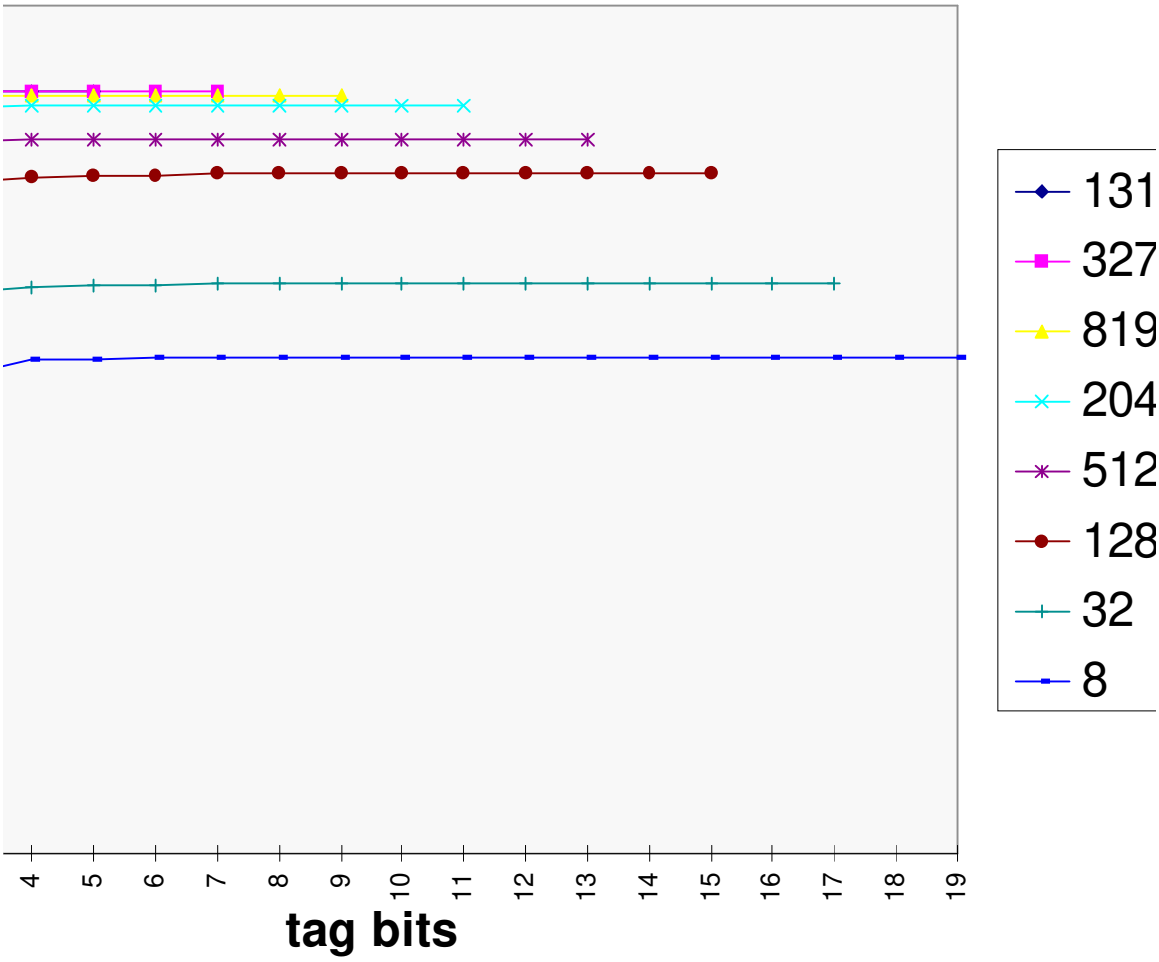
rsion of ‘xsim’, written in C++, SGI/Ir

xified’ object file, produces BTB statis

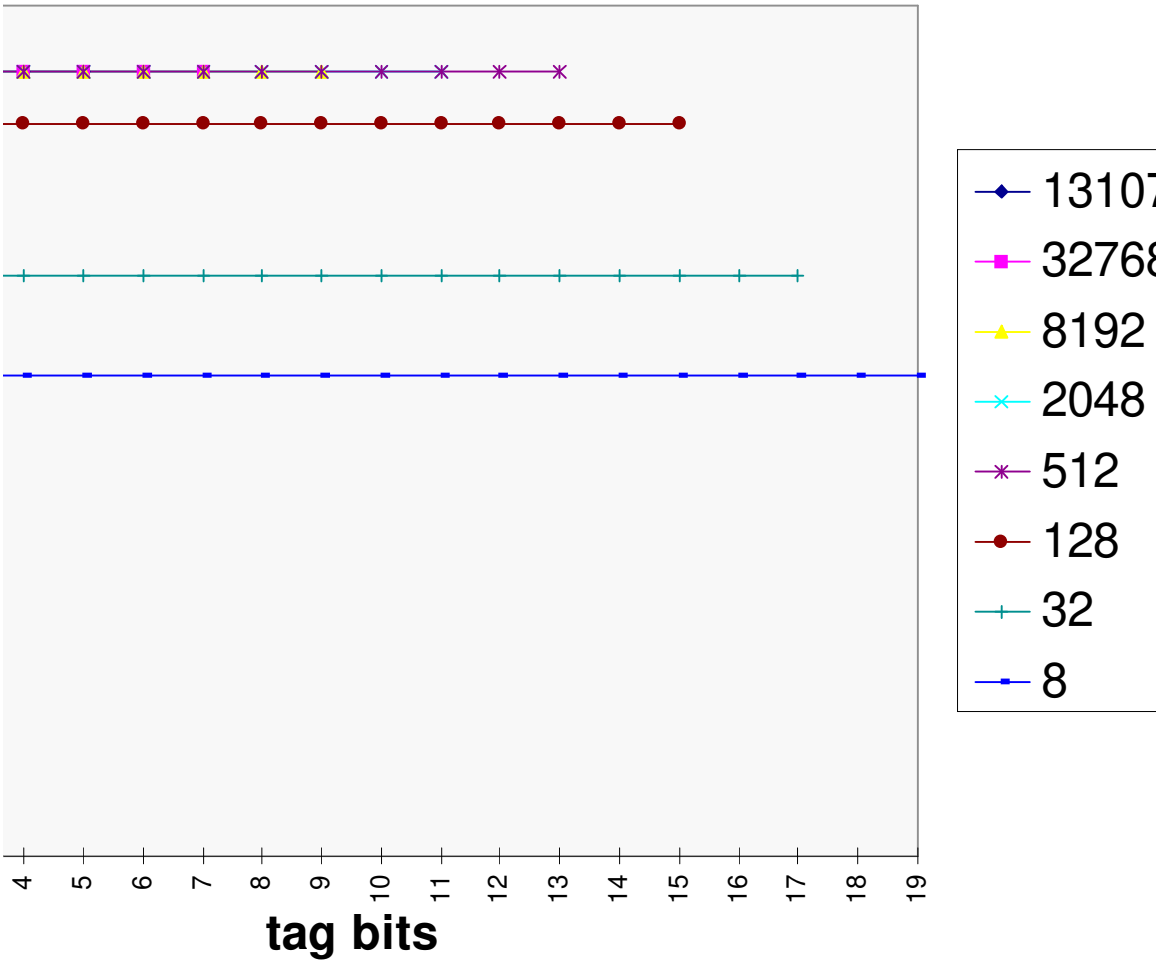
l BTB accesses by type, 1,2 & 4-way
, sizes from 8 entries up to 2M. “Fore
Hill and Smith, extended to support p

here is for direct mapped BTBs only.

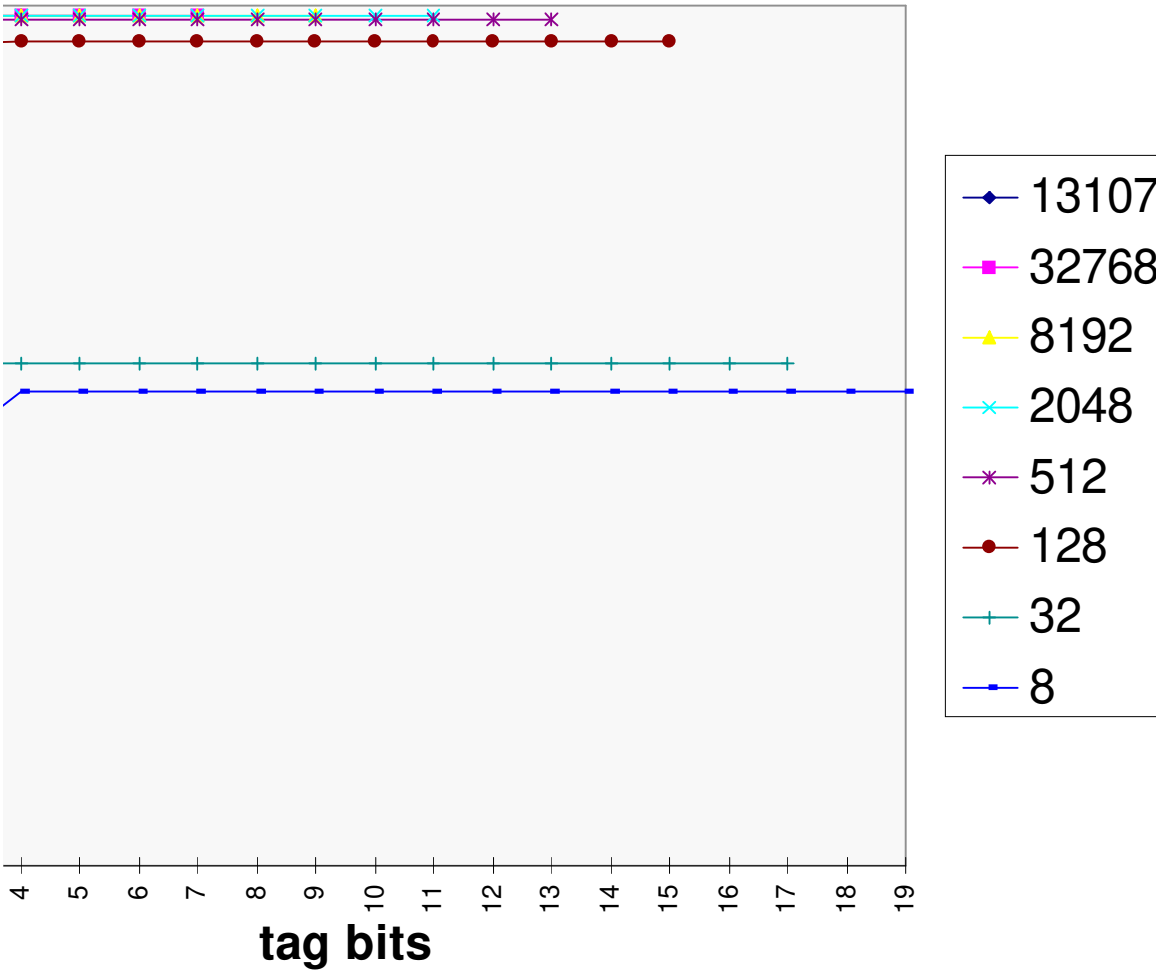
Prediction accuracy: SPEC



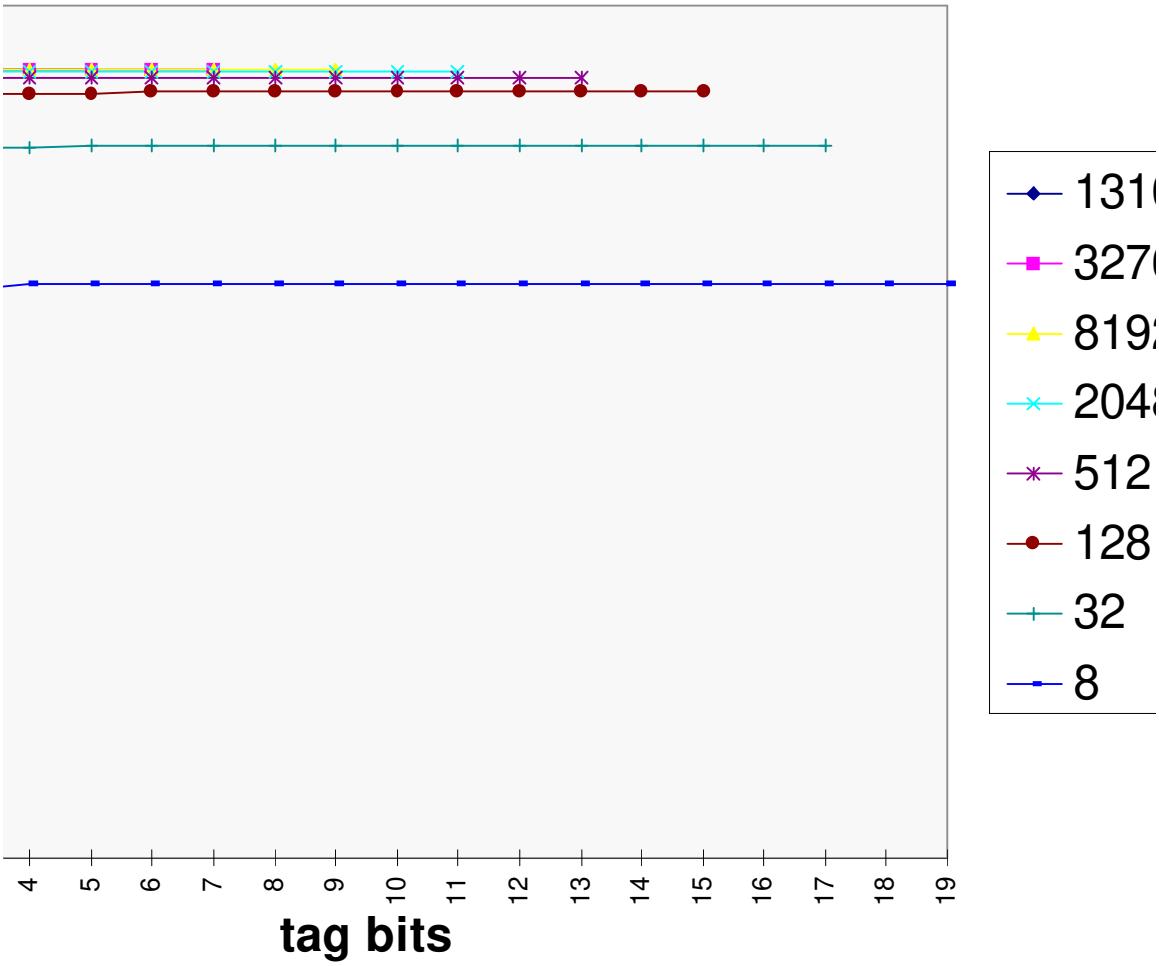
Prediction accuracy: COMPRESS



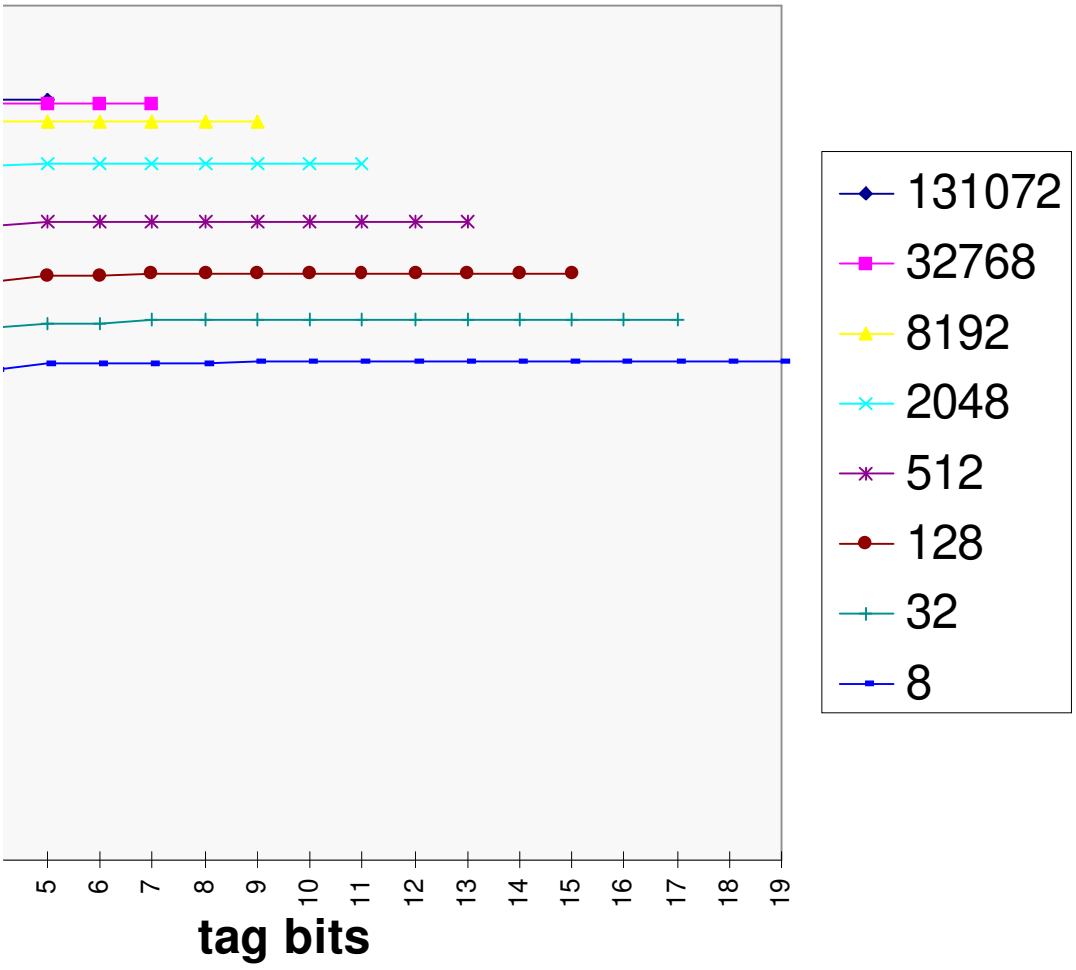
Prediction accuracy: EQNTOTT



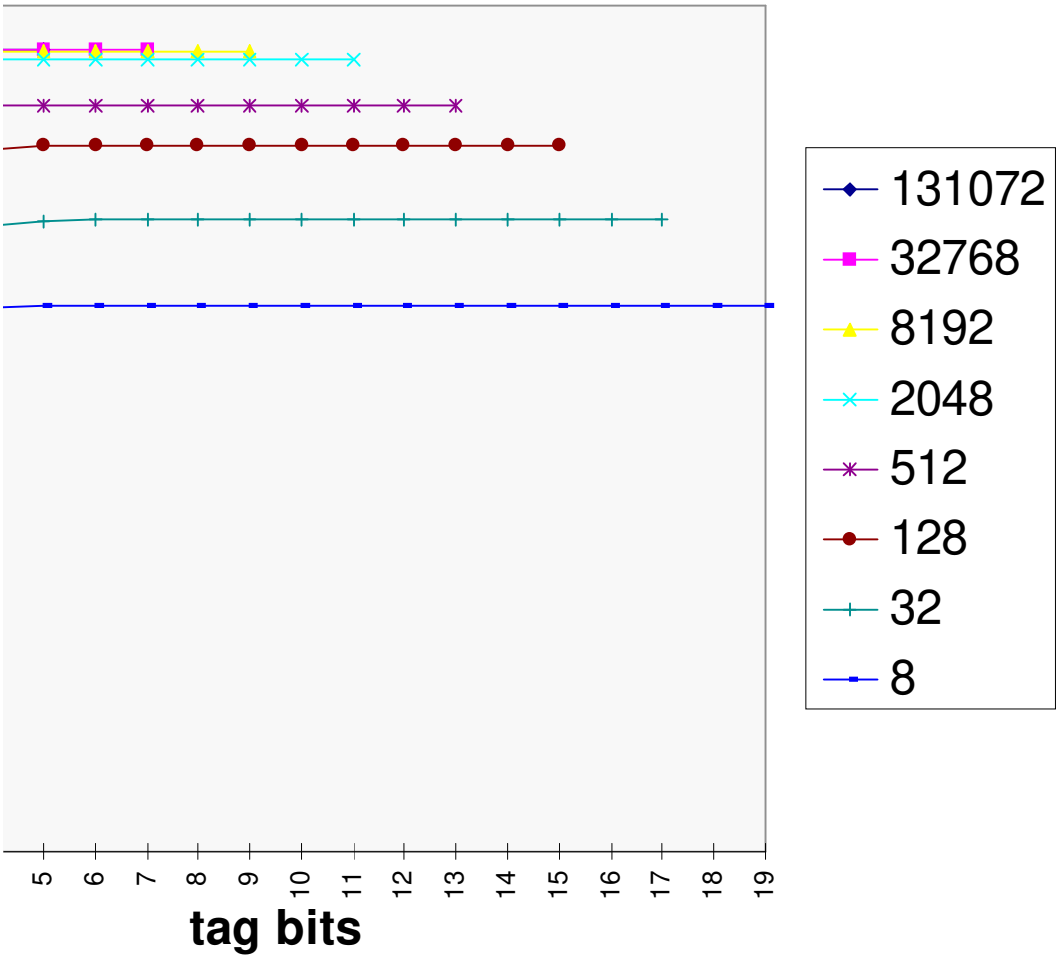
Prediciton accuracy: ESPRESSO



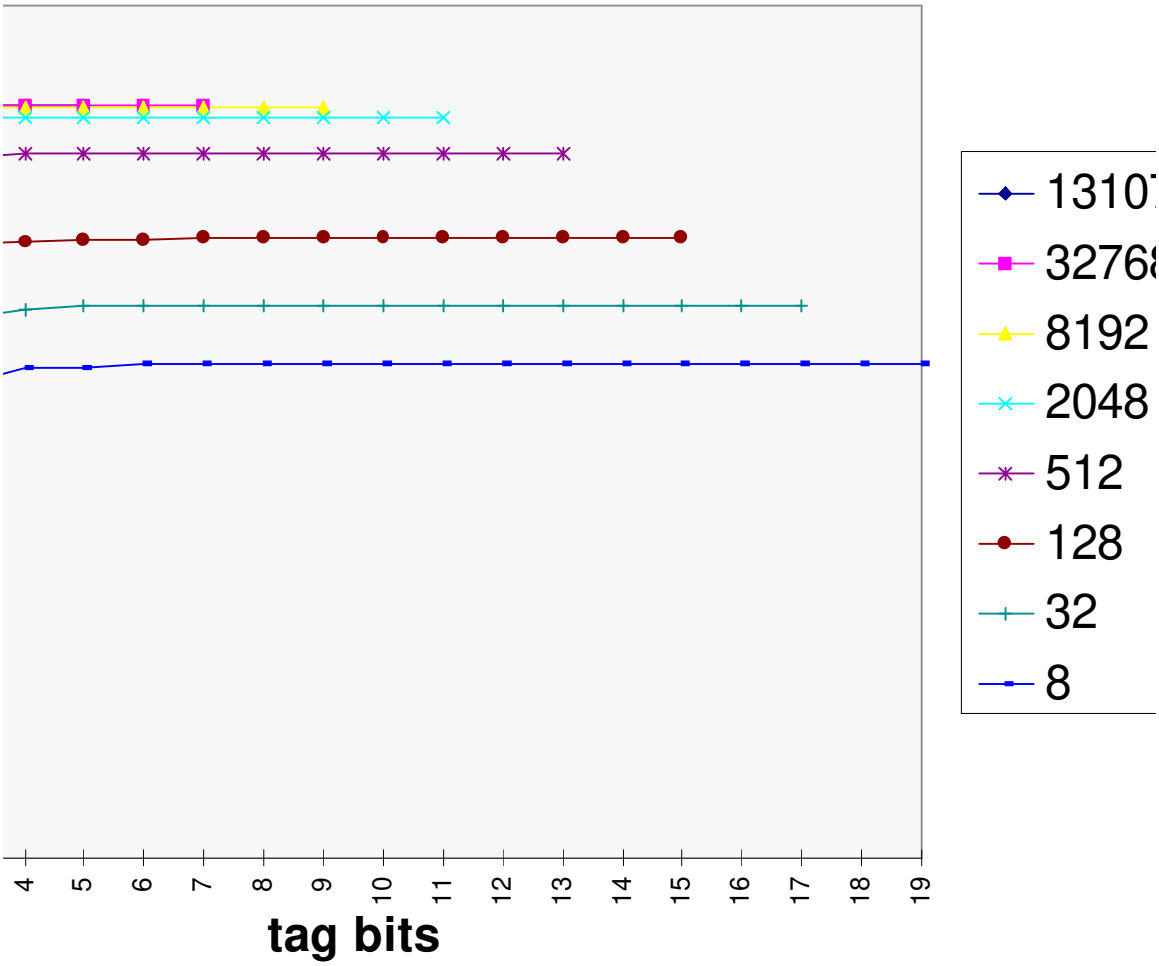
Prediction accuracy: GCC



Prediction accuracy: SC



Prediction accuracy: XLISP



	# TAG BITS NEEDED FOR 99.9% OF FULL TAG BIT ACCURACY					# TAG BITS NEEDED FOR 99.99% OF FULL TAG BIT ACCURACY				
MARK	BTB SIZE					BTB SIZE				
	8	32	128	512	2048	8	32	128	512	2048
	3	3	2	0	0	3	3	2	0	0
	4	3	2	0	0	4	4	2	0	0
	3	3	3	1	0	5	4	4	4	3
	5	7	6	5	4	8	9	7	7	6
	5	5	5	4	2	7	6	6	6	4
	6	5	5	4	2	6	7	7	6	4
	3	3	2	0	0	3	3	2	0	0
	6	5	5	4	2	7	6	6	6	4
	4	4	4	2	1	5	5	5	4	3

ag Bits Required for at least 99.9% and 99.99% of Maximum Accuracy For Individual Benchmarks

BTB Size

8	32	128	512	2K	8K	32K	128K
7	7	5	4	2	1	1	1
9	9	7	5	3	1	1	1
11	11	9	7	5	3	1	1
13	11	11	9	7	5	3	1
12	11	9	7	5	3	1	1
8	8	8	6	4	2	1	1

mum Effective BTB Tag Bits

ons

ndicate that considerable sav
width can be achieved
g performance.

e 99.99% of full tag accurac
9 tag bits for 512 entry BTB.

croprocessors can benefit: AM
M32, Intel Pentium and P6.

ork

hmarks, SPEC95 suite

ion of other architectures

quantitative estimates of area

ıms for efficient simulation of

l