ADVANCE PROGRAM

MICRO-28

The 28th Annual IEEE/ACM International Symposium on Microarchitecture

with special emphasis on
Instruction-Level Parallel Processing

Sponsored by **IEEE TC-MICRO** *and* **ACM SIGMICRO**

Ann Arbor, Michigan
November 29 - December 1, 1995

This and other conference information (including talk abstracts) can be accessed via World Wide Web at **http://american.cs.ucdavis.edu/Micro28** or by anonymous ftp from **american.cs.ucdavis.edu:/Micro28** or by sending e-mail to **micro28@cs.ucdavis.edu**.

Conference at a glance

Tuesday, November 28

18:30-20:00 Welcoming Reception

Wednesday, November 29

08:00-08:15 Welcoming Remarks:
08:15-09:15 Keynote Address:
Richard I. Baum, IBM
09:30-10:45 Session 1: Branch Prediction I
11:00-12:15 Session 2: ILP Compilation I
13:45-15:00 Session 3: Memory System Issues
15:15-16:15 Session 4: Software Pipelining and ILP Compilation
20:00-22:00 Business Meeting

Thursday, November 30

08:00-09:00 Invited Speaker:
Thomas A. Jermoluk, SGI
09:15-10:05 Session 5: Data Flow and Multi-threading Architectures
10:20-11:35 Session 6: ILP Compilation II
11:50-12:20 Session 7: Analysis of Branching Architecture
13:45-14:35 Session 8: Software and Hardware Object Code Translation
15:00-15:45 Session 9: Data Prefetching
16:00-17:30 Panel: "The Best Road to Higher Performance: VLIW vs SMP vs Superscalar vs Multiscalar vs ..."
19:00-21:30 Conference Dinner

Friday, December 1st

08:00-09:00 Invited Speaker: Fred J. Pollack, Intel
09:15-10:00 Session 10: Branch Prediction II
10:15-11:00 Session 11: Multithreading and Superscalar Design Studies
11:15-12:30 Session 12: Architectural Features for ILP
12:30-13:30 Conference Luncheon
13:45-15:00 Session 13: Software Pipelining II
15:00-15:15 Closing Remarks

Saturday, December 2

Tutorials: Intel P6, HaL SPARC64, HP PA8000
Organizer: Yale Patt, University of Michigan

Tutorials

The MICRO-28 tutorials will feature three 2 1/2 hour presentations on the microarchitectures and the sets of rationale behind the major design decisions of three important new microprocessors. All of them have been announced since the last Micro symposium.

The three have been selected due to the breadth of their target ISAs, in addition to their importance in the relevant segments of the marketplace. The three are Intel's P6 (the latest of the x86 implementations), HaL's SPARC64 (the latest of the SPARC 64 bit implementations), and Hewlett-Packard's PA8000 (one of the latest of the new RISC implementations).

The presentations will be given by distinguished technical experts from each of the three companies. Each speaker was centrally involved with the design of his company's respective chip.

The tutorials will be provided free of charge to the registrants of MICRO-28.

Conference Officials

General Chair	**Program Chair**	**Publicity Chair**
Trevor Mudge	Kemal Ebcioglu	Matthew Farrens
University of Michigan	*IBM T.J. Watson*	*UC Davis*

Steering Committee

Richard Belgard *Consultant*	James Bondi *Texas Instruments*	Matthew Farrens *UC Davis*
Wen-mei Hwu *Illinois*	Gearold Johnson *National Tech'l U.*	Hans Mulder *Intel*
Yale Patt *Michigan*	Andrew Wolfe *Princeton*	

Program Committee

Vicki Allan *Utah State*	Richard Belgard *Consultant*	David Bernstein *IBM Israel*
James Bondi *Texas Instruments*	Bob Colwell *Intel*	Henk Corporaal *Delft University*
Jim Dehnert *Silicon Graphics*	Josh Fisher *HP Labs*	Mike Flynn *Stanford*
Guang Gao *McGill U.*	Jean-Luc Gaudiot *USC*	Rajiv Gupta *Pittsburgh*
Stanley Habib *CUNY*	Martin Hopkins *IBM TJ Watson*	Wen-mei Hwu *Illinois*
Monica Lam *Stanford*	Mill Mangione-Smith *UCLA*	Steve Melvin *Zytek*
Maime Moreno *IBM TJ Watson*	Alex Nicolau *UC Irvine*	Yale Patt *Michigan*
Bob Rau *HP Labs*	Vivek Sarkar *IBM*	John Shen *CMU*
Gabriel Silberman *IBM TJ Watson*	Jim Smith *Wisconsin*	Mike Smith *Harvard*
Mary Lou Soffa *Pittsburgh*	Andrew Wolfe *Princeton*	

TUESDAY, NOVEMBER 28

18:30-20:00 Welcoming Reception

WEDNESDAY, NOVEMBER 29

08:00-08:15 Welcoming Remarks:
Trevor Mudge, *General Chair*
Kemal Ebcioglu, *Program Chair*

08:15-09:15 Keynote Address: Richard I. Baum, *IBM*

09:30-10:45 Session 1: Branch Prediction I
Session Chair: Yale Patt, Michigan

- "Performance Issues in Correlated Branch Prediction Schemes", *Nicolas Gloy, Michael D. Smith, Cliff Young - Harvard*
- "Dynamic Path-Based Branch Correlation", *Ravi Nair, IBM T.J. Watson Research Center*
- "The Predictability of Libraries", *Brad Calder, Dirk Grunwald - University of Colorado, Boulder, and Amitabh Srivastava, DEC Western Research Lab*

11:00-12:15 Session 2: ILP Compilation I
Session Chair: Guang Gao, McGill University

- "The Performance Impact of Incomplete Bypassing in Processor Pipelines", *Pritpal S. Ahuja, Douglas W. Clark, Anne Rogers - Princeton University*
- "Efficient Instruction Scheduling Using Finite State Automata", *Vasanth Bala - HP Labs, Norman Rubin, DEC*
- "Critical Path Reduction for Scalar Programs", *Michael Schlansker, Vinod Kathail - HP Labs*

13:45-15:00 Session 3: Memory System Issues
Session Chair: Andrew Wolfe, Princeton

- "A Limit Study of Local Memory Requirements Using Value Reuse Profiles", *Andrew S. Huang, John P. Shen - Carnegie Mellon University*
- "Zero-Cycle Loads: Microarchitecture Support for Reducing Load Latency", *Todd M. Austin, Gurindar S. Sohi - University of Wisconsin, Madison*
- "A Modified Approach to Data Cache Management", *Gary Tyson - UC Riverside, Matthew Farrens, John Matthews - UC Davis, Andrew Pleszkun - University of Colorado, Boulder*

15:15-16:15 Session 4: Software Pipelining and ILP Compilation
Session Chair: Bob Rau, HP Labs

- "Petri Net versus Modulo Scheduling for Software Pipelining", *V.H. Allan, U.R. Shah, K.M. Reddy - Utah State University*
- "Modulo Scheduling with Multiple Initiation Intervals", *Nancy J. Warter-Perez, Noubar Partamian - Cal State University, Los Angeles*
- "Effective Scheduling of Directed Acyclic Graphs under Register Constraints", *Balas Natarajan, Michael Schlansker - HP Labs*
- "Improving Instruction-Level Parallelism by Loop Unrolling and Dynamic Memory Disambiguation", *Jack W. Davidson, Sanjay Jinturkar - University of Virginia*

20:00-22:00 Business Meeting

THURSDAY, NOVEMBER 30

08:00-09:00 Invited Speaker: Thomas A. Jermoluk, *SGI*

09:15-10:05 Session 5: Data Flow and Multithreading Architectures
Session Chair: Jean-Luc Gaudiot, USC

- "Self-Regulation of Workload in the Manchester Data-Flow Computer", *John R. Gurd, David F. Snelling - University of Manchester (UK)*
- "The M-Machine Multicomputer", *Marco Fillo, Stephen W. Keckler, William J. Dally, Nicholas P. Carter, Andrew Chang, Yevgeny Gurevich, Whay S. Lee - MIT AI Laboratory and Laboratory for Computer Science*

10:20-11:35 Session 6: ILP Compilation II
Session Chair: Jim Dehnert, SGI

- "Region-Based Compilation: An Introduction and Motivation", *Richard E. Hank, Wen-mei W. Hwu - University of Illinois, and B. Ramakrishna Rau - HP Labs*
- "An Experimental Study of Several Cooperative Register Allocation and Instruction Scheduling Strategies", *Cindy Norris, Lori L. Pollock - University of Delaware*
- "Register Allocation for Predicated Code" *Alexandre E. Eichenberger, Edward S. Davidson - Michigan*

11:50-12:20 Session 7: Analysis of Branching Architecture
Session Chair: Ed Davidson, Michigan

- "Branch Aliasing in Branch Target Buffers", *Barry Fagin - U.S. Air Force Academy, Kathryn Russell - Lockheed Sanders, Inc.*
- "A System Level Perspective on Branch Architecture Performance", *Brad Calder, Dirk Grunwald - University of Colorado, Boulder, Joel Emer - DEC*

13:45-14:35 Session 8: Software and Hardware Object Code Translation
Session Chair: Wen-Mei Hwu, Illinois

- "Dynamic Rescheduling: A Technique for Object Code Compatibility in VLIW Architectures" *Thomas M. Conte, Sumedh W. Sathaye - North Carolina State University*
- "Improving CISC Instruction Decoding Performance Using a Fill Unit", *Mark Smotherman, Manoj Franklin - Clemson University*

15:00-15:45 Session 9: Data Prefetching
Session Chair: Gearold Johnson, National Tech

- "SPAID: Software Prefetching In Pointer and Call-Intensive Environments", *Mikko H. Lipasti, William J. Schmidt, Steven R. Kunkel, Robert R. Roediger - IBM*
- "An Effective Programmable Prefetch Engine for On-Chip Caches", *Tien-Fu Chen - National Chung Cheng University (Taiwan)*
- "Cache Miss Heuristics and Preloading Techniques for General-Purpose Programs", *Toshihiro Ozawa - Fujitsu Laboratories Ltd., Shin'ichiro Nishizaki - Fujitsu Social Science Laboratory Ltd., Yasunori Kimura - Fujitsu Laboratories Ltd. (Japan)*

16:00-17:30 Panel

Organizer: Jim Bondi, Texas Instruments
Title: "The Best Road to Higher Performance: VLIW vs SMP vs Superscalar vs Multiscalar vs ..."
Panelists:

Bill Dally (MIT)
Wen-Mei Hwu (University of Illinois)
Kunle Olukotun (Stanford University)
Yale Patt (University of Michigan)
Bob Rau (HP labs)
Richard Sites (DEC)
Jim Smith (University of Wisconsin)

19:00-21:30 Conference Dinner

FRIDAY, DECEMBER 1st

08:00-09:00 Invited Speaker: Fred J. Pollack, *Intel*

09:15-10:00 Session 10: Branch Prediction II
Session Chair: Bob Colwell, Intel

- "Alternative Implementations for Hybrid Branch Predictors", *Po-Yung Chang, Eric Hao, Yale N. Patt - University of Michigan*
- "Control Flow Prediction with Tree-Like Subgraphs for Superscalar Processors", *Simonjit Dutta, Manoj Franklin - Clemson University*
- "The Role of Adaptivity in Two-level Adaptive Branch Prediction", *Stuart Sechrest, Chih-Chieh Lee, Trevor N. Mudge - University of Michigan*

10:15-11:00 Session 11: Multithreading and Superscalar Design studies
Session Chair: Hans Mulder, Intel

- "Design of Storage Hierarchy in Multithreaded Architectures" *Lucas Roh - Argonne National Laboratory, Walid A. Najjar - Colorado State University*
- "An Investigation of the Performance of Various Instruction-Issue Buffer Topologies" *Stephan Jourdan, Pascal Sainrat, Daniel Litaize - Institut de Recherche en Informatique de Toulouse, Universite Paul Sabatier (France)*
- "Decoupling Integer Computation in Superscalar Processors" *Subbarao Palacharla, J.E. Smith - University of Wisconsin, Madison*

11:15-12:30 Session 12: Architectural Features for ILP
Session Chair: Steve Melvin, Zytek

- "Exploiting Short-Lived Variables in Superscalar Processors", *Luis A. Lozano C., Guang R. Gao - McGill University (Canada)*
- "Partitioned Register File for TTAs", *Johan Janssen, Henk Corporaal - Delft University of Technology (Netherlands)*
- "Disjoint Eager Execution: An Optimal Form of Speculative Execution", *Augustus K. Uht, Vijay Sindagi - University of Rhode Island*

12:30-13:30 Conference Luncheon

13:45-15:00 Session 13: Software Pipelining II
Session Chair: Stanley Habib, CUNY

- "Unrolling-Based Optimizations for Software Pipelining", *Daniel M. Lavery, Wen-mei W. Hwu - University of Illinois*
- "Stage Scheduling: A Technique to Reduce the Register Requirements of a Modulo Schedule", *Alexandre E. Eichenberger, Edward S. Davidson - University of Michigan*
- "Hypernode Reduction Modulo Scheduling", *Josep Llosa, Mateo Valero, Eduard Ayguade, Antonio Gonzalez - Universitat Politecnica de Catalunya. Barcelona (Spain)*

15:00-15:15 Closing Remarks

SATURDAY, DECEMBER 2

Tutorials: Intel P6, HaL SPARC64, HP PA8000
Organizer: Yale Patt, University of Michigan

MICRO-28 Registration Information

Registration

Early registration must be postmarked by November 8, 1995. Full payment in U.S. dollars must accompany registration: check drawn from a U.S. bank or charge to a MasterCard or Visa card. Credit card registrations may be faxed to (313) 763-4617, attn: Paula Denton. Conference registration includes one copy of the proceedings, lunch, reception, dinner, and coffee breaks. The student registration fee does include all meals. Student registration must include a copy of a valid, full-time student ID.

Conference Site and Accomodation

All technical sessions and lunch on Friday will be held at the Rackham Auditorium, located in the heart of the University of Michigan Campus. Pre-registration on Tuesday night will occur at the Campus Inn.

We recommend attendees stay at either the Campus Inn or the Bell Tower Hotel. Both are owned by the same company and are within two blocks of Rackham Auditorium. Please contact the hotel directly for reservations and indicate MICRO-28 conference. Conference rates at the Campus Inn are $70 per night for single rooms and $87 for double rooms. At the Bell Tower, rooms are $89 per night for single rooms and $101 for double rooms. Both hotels include continental breakfasts each morning in the price of the room. Reservations must be received by November 3, 1995, to guarantee conference rate. Late reservations will be accepted on a space-available basis.

Both hotels are on the main campus of the University of Michigan and are within walking distance of many museums, theaters, bookstores, music stores, restaurants, and bars.

Campus Inn
E. Huron & State St.
Ann Arbor, MI 48104
Call (800) 666-8693 for reservations

Bell Tower Hotel
300 S. Thayer
Ann Arbor, MI 48104
Call (800) 999-8693 for reservations

Ground Transportation

Ann Arbor is approximately 30 miles from Detroit Metro Airport. Taxi fare one way is approximately $35.00. "Commuter Transportation" is also available, which costs $15 one way ($27 round trip). It leaves every hour on the hour, and runs from 7AM to midnight. No reservations are necessary. They can be reached at 1-800-488-7433 if you need further information.

Weather

To say the weather is variable in late November is something of an understatement. Some days are beautiful and warm, others freezing and damp - it could be anywhere from 10 to 60 degrees Fahrenheit. It is more likely that it will be quite cool, however, so it is best to bring a warm coat.

Ann Arbor and Surrounding Area

With more than a hundred parks, an Arboretum and Botanical Gardens, it is easy to understand why Ann Arbor has been penned "Tree City, USA." There are over 200 restaurants in the City as well as every type of musical and sporting event that can be imagined - and it's all within walking distance of the University of Michigan campus.

MICRO-28 Registration Form
November 29 - December 1, 1995
Ann Arbor, Michigan

Name _____

Affiliation _____

Address

_____

Telephone _____

Fax _____

Electronic
Mail Address _____

☐ ACM ☐ IEEE Member Number

Please list any special needs or accommodations:_____

_____

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	Before Nov. 8	After Nov. 8
Member	$285	$345
Non-member	$360	$430
Student*	$150	$200

* Student registration must be accompanied by a copy of a valid, full-time student ID; also see the student travel grant program.

☐ Check drawn on U.S. bank payable to: **MICRO'28**

☐ Mastercard ☐ Visa

Card No._____

Expiration Date _____

Name on Card _____

Signature _____

Send or Fax registration form with payment to:

MICRO-28
c/o Paula Denton
2114A EECS Dept.
University of Michigan
1301 Beal Ave.
Ann Arbor, MI 48109-2122
Fax: (313) 763-4617

Student Travel Grant Information

I am pleased to announce the availability of MICRO-28 student travel grants. The grant program is made possible through generous donations from IBM, Texas Instruments, and Intel. The purpose of the grant is to supplement the advisors' research grants or the students' fellowship travel allowance to make attending MICRO-28 more affordable. The details of the grant are given below:

1. Students who are presenting papers at MICRO-28 will be given higher priority in the selection process. We expect to have at least 25 recipients this year.
2. We are aiming at covering approximately 50% of the airfare, hotel, and registration expenses with a maximum of $500.
3. Student applicants should fill out the enclosed application form and e-mail the application to paulad@eecs.umich.edu by November 1, 1995. The receipt of the application will be acknowledged immediately. The decision will be sent to the applicants by November 8, 1995.
4. The grant checks will be sent to the recipients AFTER the conference. Each grant recipient is required to send in all expense receipts Paula Denton at the address listed above, as well as a two-page summary of his/her experience with MICRO-28 after the conference via e-mail to paulad@eecs.umich.edu. The check will be delivered after we receive the receipts and the report.
5. The grant recipients are still required to pay the conference registration fee. Note that all student participants will be entitled to ALL MICRO-28 events and proceedings in spite of the lower registration fee for students.

Trevor Mudge
General Chair, MICRO-28

MICRO-28 Student Travel Grant Application Form

Name:_____

Affiliation: _____

Expected degree and graduation date:_____

Area of research: _____

Name of advisor: _____

Postal address for sending the grant check:_____

_____

_____

E-mail address: _____

Paper title (if presenting a paper at MICRO-28): _____

_____

Have you published at MICRO before? If so, please list years:

_____

Estimate of expenses:

airfare_____

hotel _____

registration _____

Information on the Keynote and Invited Speakers

Richard I. Baum (keynote speaker), IBM Fellow and Vice President, Systems Architecture and Performance Systems Technology and Architecture Division IBM Corporation

Dr. Baum's current responsibilities in IBM are leading the creation of strategy, design and architecture for server systems and microprocessors, and the performance modeling and analysis for microprocessor systems. These include the design and analysis of future products and the development of underlying technologies needed for them.

Dr. Baum joined IBM as a Senior Associate Programmer in the MVS Design group in the Poughkeepsie Programming Center in 1976, advanced to Development Manager in 1979, and then to Senior Programmer Manager in 1982. From 1984 to 1985 he was Technical Assistant to the Poughkeepsie Site General Manager. In 1985, he was promoted to Manager of Systems Technology in the Poughkeepsie Laboratory. After assuming responsibility for Central System Architecture, High End Processor Performance and Future Systems Design, Baum became Director of System Architecture and Design in 1989, and was appointed an IBM fellow while in this assignment in 1991. In 1993, Dr. Baum was appointed Assistant General Manager, Systems Technology, and in 1994, he was appointed Vice President, Systems Architecture and Performance, his current position.

In 1971 he received his BS in Engineering Physics from Cornell, and in 1975 a PhD in Computer Science from Ohio State.

Thomas A. Jermoluk, President and Chief Operating Officer, Silicon Graphics, Inc.

Reporting directly to Edward R. McCracken, Chairman and CEO, Mr. Jermoluk is in charge of developing and delivering SGI's entire range of computing systems. He is responsible for the high and low-end IRIS workstation product groups, research and development, business development, administration, finance, business systems, operations, corporate manufacturing, customer support and marketing.

Since joining Silicon Graphics in 1986, Mr. Jermoluk has worked on the design of a new CPU and bus architecture and the corresponding UNIX operating system redesign for bringing new levels of performance to the workstation class of machines. Previously, he worked for Hewlett-Packard as a research and development section manager, responsible for hardware and software development on a new RISC-based computer. Prior to HP, he was manager of systems software at Bell Laboratories in the UNIX development lab. Mr. Jermoluk has an M.S. in computer science and a B.S. in computer science/electrical engineering from Virginia Tech.

Fred J. Pollack, Intel Fellow, Director of Measurement, Architecture, and Planning, Microprocessor Products Group, Intel Corporation

Fred Pollack has worked at Intel for 18 years. He is currently the Director of the group responsible for all x86 platform architecture and performance analysis. He also directs the planning for Intel's future x86 microprocessors. Before this, he was the manager of the P6 Architecture. In January of 1993, he was promoted to an Intel Fellow, one of 9 in the company.